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Carsten Fallesen

Design Techniques for Sub-micron RF Power Amplifiers

PhD thesis

Nokia Mobile Phones
and
Department of Information Technology
Technical University of Denmark

May 2001

DTU

Design Techniques for Sub-micron RF Power Amplifiers

Carsten Fallesen

Nokia Mobile Phones

Department of Information Technology
Technical University of Denmark

Abstract

In the last couple of years there has been an increased focus on integrated RF power amplifiers for wireless communications, especially mobile phones. The drivers of the development high integration and low cost. The highest integration possible will most probably be achieved with CMOS processes. At the same time CMOS is without doubt the cheapest process available.

To be able to reach the goal some theory on RF power amplifiers is necessary. The different classes of operation are explained, then the principles of impedance matching is discussed. This includes the development of the simulated load-pull method and synthesis of impedance matching networks. Then the biasing of the power amplifier is discussed along with the stability issues.

The choice of CMOS as a preferred technology for the power amplifier is justified. The issues of modeling a complete power amplifier is treated. This includes modeling of the transistors, the passive devices on-chip and off-chip as well as the package and PCB. To ease the design of power amplifier a design method is developed based on the theory and the experimental work.

At last the experimental work is described. The first part is a linearization system based on digital predistortion. The digital predistortion can be used to increase the overall efficiency of varying envelope systems. Then three CMOS power amplifiers designed during the project are introduced. The last of these power amplifiers shows superior performance when compared to other CMOS power amplifiers. The output power of this power amplifier is 30.4dBm with a power added efficiency of 55%. The last power amplifier utilizes the design method develop as well as the models described. The accurate modeling combined with superior performance proves the future of integrated CMOS power amplifiers for wireless communication.

Resume (Danish)

I de seneste år har der været øget fokus på integrerede RF effektforstærkere til trådløs kommunikation, især mobiltelefoner. Det der har drevet udviklingen er især ønsket om høj integration og lav pris. Den højeste integration vil formentlig ske i en CMOS teknologi. Samtidigt er CMOS uden tvivl den billigste teknologi der er til rådighed.

For at nå målet er det nødvendigt at gennemgå den basale teori om RF effektforstærkere. De forskellige klasser af forstærkere bliver forklaret, efterfølgende bliver teorien bag impedans tilpasning diskuteret. Dette inkluderer udviklingen af en metode til simuleret load-pull og syntese af impedans tilpasnings netværk. Derefter bliver biasing af effektforstærkere diskuteret sammen med stabilitet af effektforstærkere.

Valget af CMOS som den fortrukne teknologi til effektforstærkere bliver begrundet. Spørgsmålene omkring modellering af komplette effektforstærkere bliver behandlet. Dette inkluderer modellering af transistorerne, de passive komponenter på og udenfor den integrerede kreds såvel som pakken og printkortet. For at lette udviklingen af effektforstærkere er en design metode blevet udviklet baseret på både teorien og det eksperimentelle arbejde.

Til sidst bliver det eksperimentelle arbejde beskrevet. Den første del er et linearisering system baseret på digital predistortion. Den digitale predistortion kan bruges til at øge effektiviteten i systemer med varierende amplitude. Efter det bliver tre CMOS effektforstærkere der er blevet udviklet i løbet a projektet beskrevet. Den sidste af disse effektforstærkere udviser bedre egenskaber end nogen anden CMOS effektforstærker. Denne effektforstærker giver en udgangseffekt på 30.4dBm med en effektivitet på 55%. Den sidste effektforstærker blev udviklet ved hjælp af den nye design metode sammen med de modeller der bliver beskrevet. Den præcise simulering sammen med de uovertrufne egenskaber demonstrerer fremtiden i integrerede CMOS effektforstærkere til trådløse produkter.

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Glossary

ACP	Adjacent channel power
ACPR	Adjacent channel power ratio
AMPS	Advanced mobile phones system
CAD	Computer aided design
CDMA	Code division multiple access
CMOS	Complementary metal-oxide-semiconductor
COB	Chip on board
DSP	Digital signal processor
DSV	Dynamic supply voltage
GaAs	Gallium Arsenide
GMSK	Gaussian minimum phase shift keying
GSM	Global system for mobile communications
HBT	Heterojunction bipolar transistor
IMD	Intermodulation distortion
LDMOS	Laterally diffused MOS
MOSFET	Metal oxide semiconductor field effect transistor
MESFET	Metal semiconductor field effect transistor
OQPSK	Offset quadrature phase shift keying
PAE	Power added efficiency
PCB	Printed circuit board
QPSK	Quadrature phase shift keying
RFC	RF choke
SAR	Specific absorption rate
SiGe	Silicon Germanium
SMD	Surface mount device
SOI	Silicon on insulator
TDMA	Time division multiple access
UMTS	Universal mobile telephone system
W-CDMA	Wideband code division multiple access

Errata

p.4, eq. 1.4 **P_{ch} is the power in the channel, while P_{adj} is the power in the adjacent channel**

p. 10, l. 9 ***output impedance*** **should be** ***load impedance***

p. 17, l. 3 ***power added efficiency*** **should be** ***output power***

p. 28, eq. 3.19

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

p. 37, l. 15 **the impedance** ***10 - j10*** **should be** ***10 - j15***

p. 41, fig 3.21 **The gain in Fig 3.21 has not been normalized and the maximum should be 0dB**

CHAPTER 1
INTRODUCTION

Over the last couple of years there has been an increasing focus on highly integrated high efficiency power amplifiers for wireless communication systems, especially mobile phones. This is also the topic of this thesis.

In the first chapters of this thesis the basic theory is explained. Then the concept of simulated load-pulling is introduced in conjunction with automated impedance matching network synthesis. This is followed by a comparison of semiconductor technologies with focus on CMOS. Then the modeling of active and passive components is described. A number of experimental CMOS power amplifiers were constructed during the project and the results of these are presented at last.

The design of power amplifiers in the past did not follow a stringent design method, it rather seemed like black magic was performed. In this thesis a design method is developed based on the basic theory of power amplifier design and this is used to formalize the design process.

In the last part of this thesis experimental results on CMOS power amplifiers as well as a digital linearizations system is presented. The CMOS power amplifiers show results better than any other CMOS power amplifier presented so far, the results are even comparable to commercial power amplifiers in more exotic technologies.

In the remainder of this chapter the basic definitions used in conjunction with power amplifiers will be explained.

1.1 Basics of RF Power Amplifiers

A simple power amplifier is illustrated in Figure 1.1. The power amplifier consists of an input impedance matching network, an amplifying stage and an output impedance matching network. Furthermore DC bias is applied at the input and output ports of the amplifying stage [1][2].

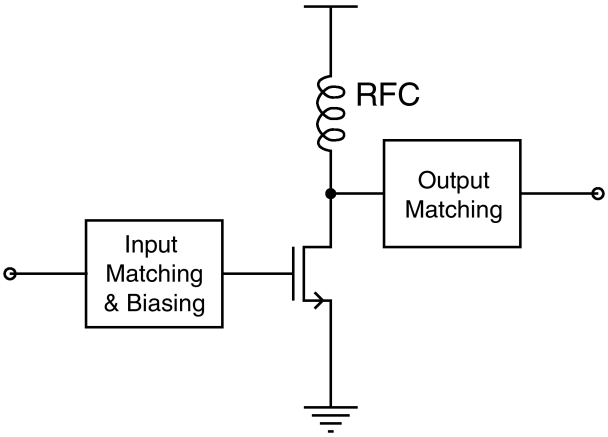

Figure 1.1 Simple power amplifier.

The power amplifiers can be divided into narrowband and broadband power amplifiers. In most communication systems narrowband power amplifiers are used, since they are usually more efficient than the broadband amplifiers.

The power amplifier has a number of characteristic properties that will now be explained. First of all the power gain of a power amplifier is defined as the output power divided by the input power:

$$G = \frac{P_{out}}{P_{in}} \qquad \textbf{(1.1)}$$

In practice most power amplifiers will be multistage amplifiers to obtain sufficient power gain. The combination of several stages often introduces problems with stability of the power amplifier due to the increased gain from input to output. The principle of a two-stage power amplifier is shown in Figure 1.2.

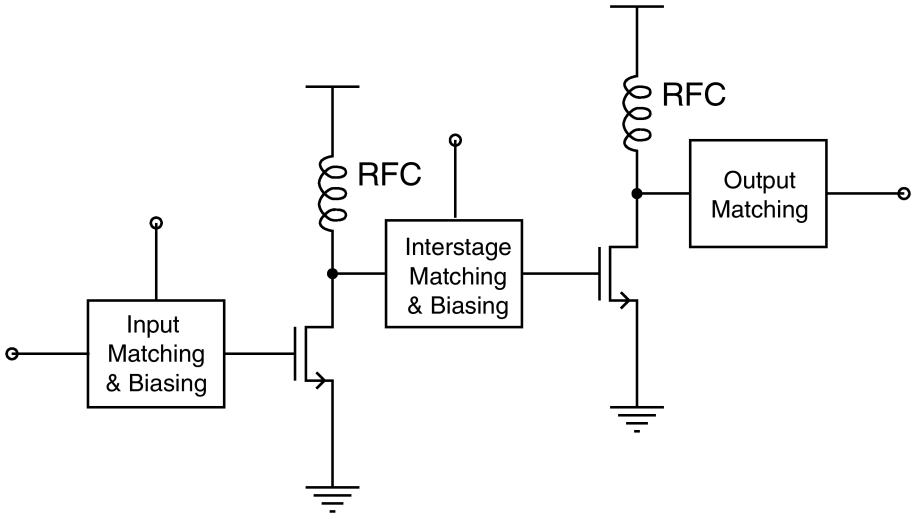

Figure 1.2 Principle of a two-stage power amplifier.

1.1.1 Definitions of Efficiency

The efficiency is probably the most important property of the power amplifier, since a very large part of the total power dissipated in a mobile phone is dissipated in the power amplifier. The efficiency is limited by the selected class of operation and the parasitic components, as described in chapter 2. The efficiency can be expressed as either drain efficiency or power added efficiency. The drain efficiency is given by:

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} \tag{1.2}$$

On the system level the efficiency of the driver stages is also important, and then the power gain of the power amplifier must be included. The power gain of a power amplifier is also dependent upon the class of operation, as well as the chosen technology. Different classes of operation have different relative power gains. The inclusion of the power gain leads to the expression for power added efficiency:

$$\eta_{add} = \frac{P_{out}-P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}} \cdot \left(1 - \frac{1}{G}\right) \tag{1.3}$$

The power added efficiency is more relevant to the system designer than the drain efficiency, but as mentioned above this depends highly of the technology. It is therefore difficult to compare two classes of operation, without knowing the properties of the power transistor.

1.1.2 Definitions of Linearity

One of the other important parameters in power amplifier design is the nonlinearity of the power amplifier. The nonlinearity originates from the active components. If the wireless communication system utilizes a varying envelope modulation the nonlinearities will cause spectral regrowth which will pollute the neighboring channels.

Gain Compression

Gain compression describes the phenomenon, when the relationship between the input and output power levels is no longer linear. When the output power is 1dB less than expected by the linear relationship the so-called 1dB Gain Compression Point (P_{1dB}) is reached. The gain compression is also known as AM-AM conversion.

AM-PM Conversion

The AM-PM conversion is caused by the phase shift of the power amplifier caused by the amplitude of the signal. This can for instance be caused by the non-linear drain-source capacitance of the MOSFET.

Intermodulation Distortion

The harmonic distortion is caused by the nonlinear active components of the amplifier. The result is distortion components at integer multiples of the signal frequency.

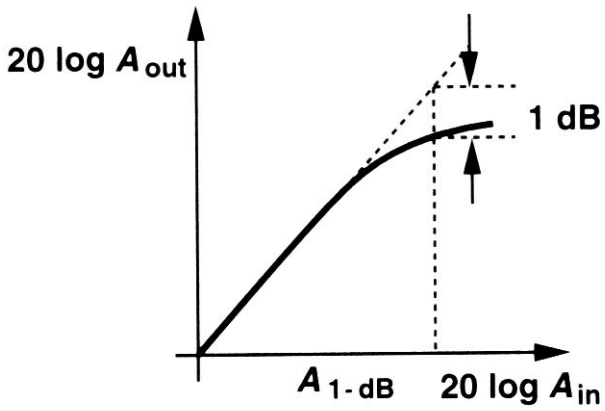

Figure 1.3 Output power as a function of input power [3].

Intermodulation distortion (IMD) is generated when more than one signal is present on the input. The intermodulation distortion is also caused by the nonlinearities of the amplifier. New third-order signals are generated at e.g. $2f_1 - f_2$ and $2f_2 - f_1$. The third-order products increase by 3 dB when the input signals increase by 1 dB. The point at which the extrapolated power levels of the third-order products reach the wanted power is called the Third-order Intercept Point (P_{3IP}). Although third-order distortions will probably be the most important a number of other orders may also be significant.

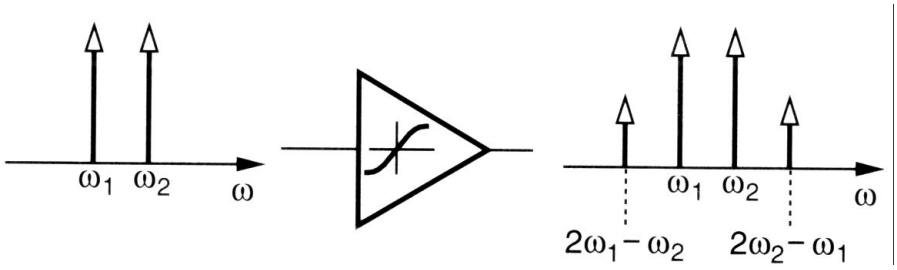

Figure 1.4 Third-order intermodulation products [3].

Adjacent Channel Power Ratio

The adjacent channel power ratio (ACPR) is one of the most important ways of characterizing the nonlinearity of a power amplifier in linear communication standards.

$$\text{ACPR} = \frac{P_{adj}}{P_{ch}} \qquad \textbf{(1.4)}$$

In Figure 1.5 a typical spectrum showing the ACPR is illustrated. The ACPR is an easy way to measure the total distortion caused by the above mentioned nonlinearities.

1.2 Mobile Phone Standards

The mobile phone standards have evolved quickly over last decades. The first standards used continuos time frequency modulation (FM), now wideband code division multiple access (W-CDMA) or time division multiple access (TDMA) systems with quadrature

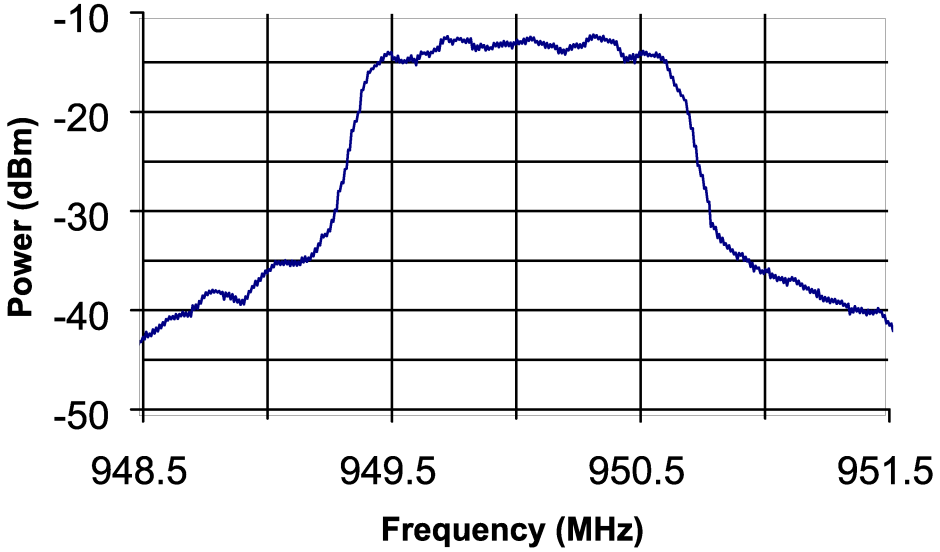

Figure 1.5 Spectrum showing ACPR measurement.

modulation formats are being deployed. In the following sections the most important features of the three generations introduced until now will be described.

1.2.1 First Generation

The first generation mobile phone standards employed analog modulation formats. The first systems were used in USA in the 1950s. One of the most successful first generation standards was the Nordic Mobile Telephone standard (NMT), developed in the nordic countries in the early 1980s. This standard served as an example of the importance of roaming across countries and different network operators.

A few of the first generation systems are still in use most notably the NMT and the north-american Advanced Mobile Phone System (AMPS). Since these systems are all FM systems, the nonlinearities of the power amplifiers are not a problem.

1.2.2 Second Generation

The second generation mobile phone standards all use digital modulation formats. The the digital modulation allows for digital data services. The main advantage of the digital modulation is however the possibility to share a single channel between several users. The sharing is done either through time division multiple access (TDMA) or code division multiple access (CDMA).

GSM-900/1800/1900

The Global System for Mobile Communications (GSM) standard is used all through Europe, as well as most of North America and some parts of the Asia-Pacific area. The GSM system employs GMSK modulation which is a constant envelope modulation. The sharing of the channel is done through time division. A constant envelope modulation uses a constant amplitude in the modulation, which means that the power amplifier can be nonlinear. The GSM system features global roaming between different operators. The

bitrate of the GSM system is 9.6 kbits/s in a standard system, but changing the error coding and using more than one timeslot up to 43.2 kbits/s has been achieved.

EDGE

The EDGE standard was originally developed as an extension for GSM only, but has now been integrated in other standards as well. The EDGE standard uses a modified 8PSK modulation, which is not constant envelope. The new modulation means that the nonlinear power amplifiers can no longer be used. The EDGE standard allows for bitrates up to 384 kbits/s.

The linearity requirements of the EDGE standard is expressed in terms of ACPR. In the adjacent channel the ACPR must be better than -30dBc while in the alternating channel the ACPR must be better than -54dBc. Since nonlinearities are also introduced in the circuits prior to the power amplifier then specifications for the power amplifier will typically be even harder. The ACPR is measured with a 30 kHz resolution bandwidth at the center of the channels.

IS-95 CDMA

The IS-95 standard is used primarily in North America as well as some places in the Asia-Pacific area. The IS-95 system uses QPSK modulation which utilizes varying envelope, the sharing of the channel is achieved through code division [3].

While the number of simultaneous users on a channel in a TDMA systems is determined by the number of timeslots, the number of simultaneous users in IS-95 is determined by the noise level in the channel. The noise level is optimized through aggressive power control to maximize the number of simultaneous users. Due to the power control the power amplifier has to be able to control the output power in 1dB steps over a range of 85dB.

The linearity requirements of the IS-95 standard is also expressed as ACPR. The ACPR of the adjacent channel has to be better than -42dBc, but this is for the total output power compared to a 30 kHz band, this relates to an ACPR of -26dBc.

1.2.3 Third Generation

The third generation of mobile phones is primarily focused on higher bitrates. The only serious standard until now is the Universal Mobile Telephones System (UMTS) which is a wideband CDMA system. The UMTS system will probably be the first standard with true global coverage across countries and network operators.

The UMTS standard features bitrates up to 2 Mbits/s. This bitrate will be used for multimedia applications on the mobile terminal e.g. audio and video clips. As was the case for IS-95 the power control has 1dB steps and the dynamic range is 70dB posing a real challenge for the power amplifier designer

1.3 Summary

The power amplifier is the most power consuming component in a mobile phone, and it is therefore interesting to reach higher efficiency levels for the power amplifier. There are several ways to improve the efficiency, e.g. new circuit topologies, higher level of integration and better technologies.

The linearity of a power amplifier will be an issue in future telecommunication standards, such as EDGE and UMTS. There will therefore be a need for linear power amplifiers, this can be achieved either by using linear topologies and/or linearization techniques.

The future UMTS handsets will probably contain dual-mode functionality with GSM, this means that the power amplifier must also be able to handle ordinary GSM efficiently. The dual-mode solution will be very challenging, and might not even be the optimal solution.

In this chapter the basic properties of an RF power amplifier has been defined. In the following chapters the details of the power amplifiers will be discussed. In chapter 2 the classes of operation are discussed. The trade-offs between different class of operation are discussed. The impedance matching of the power amplifier is described in chapter 3. This includes methods to obtain optimal impedance matching as well as methods for synthesizing the impedance matching networks. Chapter 4 deals with the biasing of the power amplifier. In this chapter the issues of RF and bias stability is also discussed.

In chapter 5 the implementation technologies are discussed with focus on the deep sub-micron CMOS technologies. The modeling of active and passive components on-chip as well as on the PCB is also discussed. In chapter 6 the theory is collected in a design method for integrated power amplifiers. The design method covers the complete design of a power amplifier, from specification to verification.

In chapter 7 a digital predistortion is presented, which enables the use of nonlinear power amplifiers in systems with varying envelope. The digital predistortion system was built and experimental results obtained. Three CMOS power amplifiers have been designed during the Ph.D. project. These power amplifiers are described in chapter 8. In comparison with other published CMOS power amplifiers they shows superior performance.

1.4 Acknowledgements

This Ph.D. project have been funded by Nokia Mobile Phones in Copenhagen. I have had very fruitful discussions with a number of design engineers at Nokia. I would especially like to thank Dan Rebild for an enormous support during the entire Ph.D. project.

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[3] B. Razavi, *RF Microelectronics*. Prentice Hall, 1998.

CHAPTER 2
CLASSES OF OPERATION

The different topologies for power amplifiers can be divided into a number of classes of operation. The classes have different properties with respect to e.g. linearity, efficiency and power gain.

Usually the classes A, AB, B and C are treated as distinct modes of operation, although in reality they are a continuum of biasing conditions for the same basic mode of operation. It is therefore possible to describe class A through C as a single class with different conduction angles. The analysis of class A through C is done in Section 2.1. The classes D and F can also be analyzed as one class, this analysis will be carried out in Section 2.2. The class E operation is quite different from the other classes and will be treated separately in section Section 2.3. At last the class S operation will be described in Section 2.4.

One of the important parameters of the amplifier classes is the load line, as the name implies the load of the amplifier has an influence on the load line. The other parameter that influences the load line is the quiescent bias point.

2.1 Class A through C

The class A, AB, B and C amplifiers are very similar, except for the biasing and the output matching network. The basic class A through C power amplifier is illustrated in Figure 2.1. The biasing of the output is obtained by the RF choke (RFC). To prevent a DC current from flowing a DC block (C_{DC}) is incorporated into the design. The loadline of the power amplifier is controlled by the load resistance (R_L), while the resonator (L_R, C_R) filters out the harmonics at the output. The input matching, not illustrated here, usually contains the biasing of the input, as will be described in Chapter 4.

Which of the classes the power amplifier actually operates in is defined by the quiescent drain current, which again is defined by the input bias point. Apart from the bias point of the amplifier the loadline is the most important feature. The transistor has a large impact on the selection of the loadline of the power amplifier. To optimize the

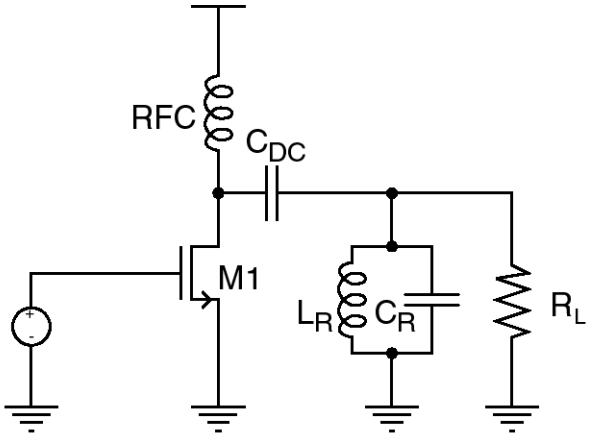

Figure 2.1 The generic setup for class A, AB, B and C amplifiers.

power amplifier, with respect to output power, efficiency or linearity, the load line should be placed correctly. When the loadline is not selected properly the power amplifier will be either current or voltage limited. The optimal load line of a power amplifier is primarily controlled by the I-V characteristic of the transistor. To obtain maximum output power the load line should be placed such that the amplifier is neither current nor voltage limited.

In the analysis of the class A through C power amplifiers it is assumed that the resonator has infinite impedance at the fundamental frequency while the impedance is zero at all other frequencies. The output impedance is defined by the load resistor (R_L). The RF choke (RFC) is ideal and allows only DC currents to flow to the transistor. Under these assumptions it is possible to derive the current and voltage waveforms at the output of the power amplifier assuming a sinusoidal drive at the input.

The analysis starts by defining the conduction angle α, which is the amount of time the transistor is conducting. Assuming a MOSFET, the conduction angle is determined by the quiescent bias voltage (V_q) on the gate of the transistor, with a corresponding quiescent current (I_q). The transistor is assumed to have a threshold voltage, below

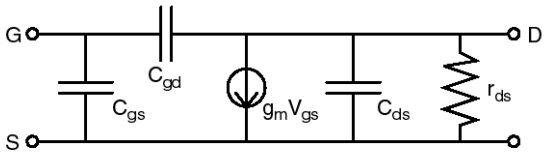

Figure 2.2 Simple RF small-signal model of MOS transistor.

which the transistor will not draw any current. The maximum current that can be drawn by the transistor is defined as I_{max}. The relation between conduction angle and bias point is shown in Figure 2.3, where biasing for 360º, and 180º conduction angles are illustrated. The selected bias points correspond to class A and B. In the same figure the ideal currents drawn by the transistor is shown.

The currents drawn by the transistor can be formulated as:

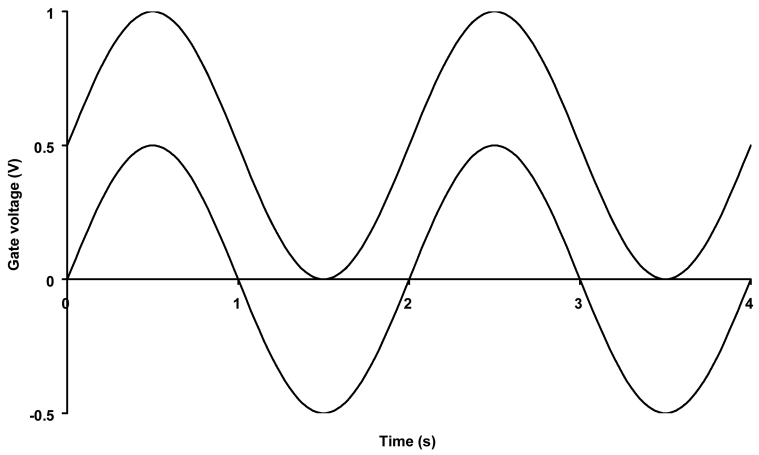

Figure 2.3 Relationship between biaspoint and conduction angle.

$$i_d(\theta) = \begin{cases} I_q + (I_{max} - I_q)\cos\theta & ,-\alpha/2 \le \theta \le \alpha/2 \\ 0 & ,-\pi < \theta < -\alpha/2; \alpha/2 < \theta < \pi \end{cases} \quad \textbf{(2.1)}$$

where

$$\cos(\alpha/2) = -\frac{I_q}{I_{max} - I_q} \quad \textbf{(2.2)}$$

isolating I_q in this equation gives:

$$I_q = \frac{I_{max}\cos(\alpha/2)}{\cos(\alpha/2) - 1} \quad \textbf{(2.3)}$$

substituting (2.3) in (2.1) gives

$$i_d(\theta) = \begin{cases} \frac{I_{max}}{1 - \cos(\alpha/2)}[\cos\theta - \cos(\alpha/2)] & ,-\alpha/2 \le \theta \le \alpha/2 \\ 0 & ,-\pi < \theta < -\alpha/2;\ \alpha/2 < \theta < \pi \end{cases} \quad \textbf{(2.4)}$$

The DC current as well as the magnitude of harmonic frequency components can be found using Fourier analysis. The DC current is then:

$$\begin{aligned} I_{dc} &= \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)}[\cos\theta - \cos(\alpha/2)]d\theta \\ &= \frac{I_{max}}{2\pi}\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1 - \cos(\alpha/2)} \end{aligned} \quad \textbf{(2.5)}$$

The magnitude of the harmonic frequency components can be found by applying Fourier analysis on the waveform described by (2.4). The magnitude of the *n*th is then:

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)}[\cos\theta - \cos(\alpha/2)]\cos n\theta d\theta \qquad \textbf{(2.6)}$$

Solving (2.6) for the fundamental frequency gives:

$$I_1 = \frac{I_{max}}{2\pi}\frac{\alpha - \sin(\alpha)}{1-\cos(\alpha/2)} \qquad \textbf{(2.7)}$$

The DC and first five harmonic currents have been plotted against the conduction angle in Figure 2.4.

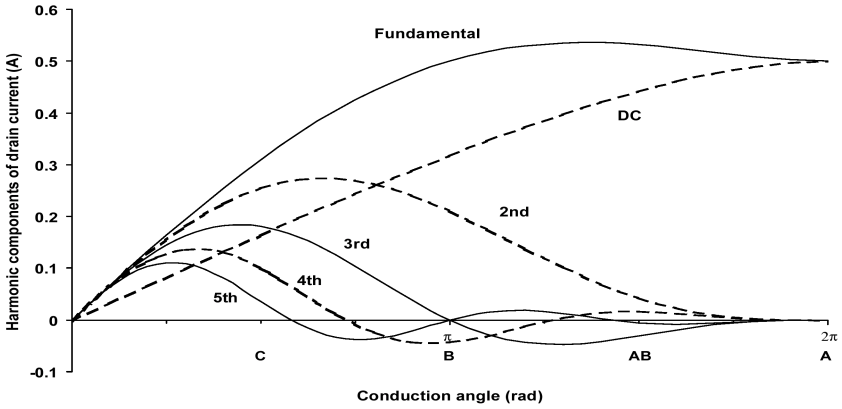

Figure 2.4 Harmonic components of current plotted as a function of conduction angle.

The power consumption and output power can now be found with the help of the the supply voltage V_{DD} and the load impedance R_L. Before the analysis the load impedance has to be defined. Assuming an ideal transistor this corresponds to:

$$R_L = \frac{V_{DD}}{I_{max}} \qquad \textbf{(2.8)}$$

This gives maximum voltage and current swing as illustrated by line (a) in Figure 2.5. The case of voltage clipping where be current swing is reduced is illustrated by line (b) while current clipping and the following reduced voltage swing is line (c).

When the load impedance is too high it corresponds to voltage clipping as illustrated by line (b). In the case of voltage clipping it is easy to see that the value of I_{max} is reduced to the effective value:

$$I_{max,\,eff} = \frac{V_{DD}}{R_L} \qquad \textbf{(2.9)}$$

When on the other hand the load impedance is too low the opposite case of current clipping occurs. This can be accounted for by using the effective voltage $V_{DD,eff}$ in place of V_{DD}.

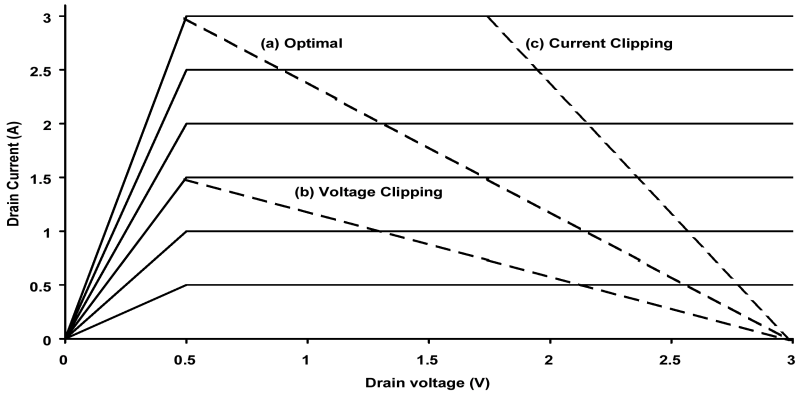

Figure 2.5 The optimal load line as well as voltage and current clipping.

$$V_{DD,\,eff} = I_{eff}R_L \tag{2.10}$$

By substituting I_{max} with I_{eff} in (2.7) the effective RF current is found:

$$I_{max,\,eff} = \begin{cases} \dfrac{V_{DD}}{R_L}, \dfrac{V_{DD}}{R_L} < I_{max} \\ I_{max}, \dfrac{V_{DD}}{R_L} \geq I_{max} \end{cases} \tag{2.11}$$

$$I_1 = \frac{I_{max,\,eff}}{2\pi}\frac{\alpha - \sin(\alpha)}{1 - \cos(\alpha/2)} \tag{2.12}$$

Using the above equations it is now possible to obtain the DC and output power of the power amplifier:

$$V_{DD,\,eff} = \begin{cases} I_{max}R_L, R_L I_{max} < V_{DD} \\ V_{DD}, R_L I_{max} \geq V_{DD} \end{cases} \tag{2.13}$$

$$P_{DC} = V_{DD}I_{DC} \tag{2.14}$$

$$P_{out} = \frac{V_{DD,\,eff}}{\sqrt{2}}\frac{I_1}{\sqrt{2}} = \frac{V_{DD,\,eff}I_1}{2} \tag{2.15}$$

it is now possible to define the drain efficiency of the power amplifier:

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} \tag{2.16}$$

it is now possible to plot the relationship between conduction angle, output power and efficiency, see Figure 2.6.

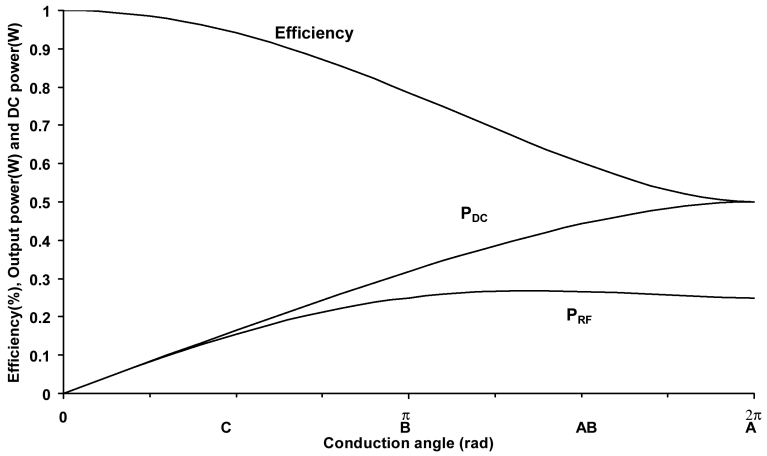

Figure 2.6 Output power, DC power and efficiency as functions of conduction angle.

2.1.1 Knee Effect

The knee effect is a property of the transistor used for the power amplifier. Due to the behavior of the MOS transistor the drain current will not only depend on the gate voltage but also on the drain voltage. This is especially noticeable at low drain voltages. The I-V characteristic of a typical submicron NMOS transistor is shown in Figure 2.7, where each of the curves represent a 0.25V increment in gate voltage.

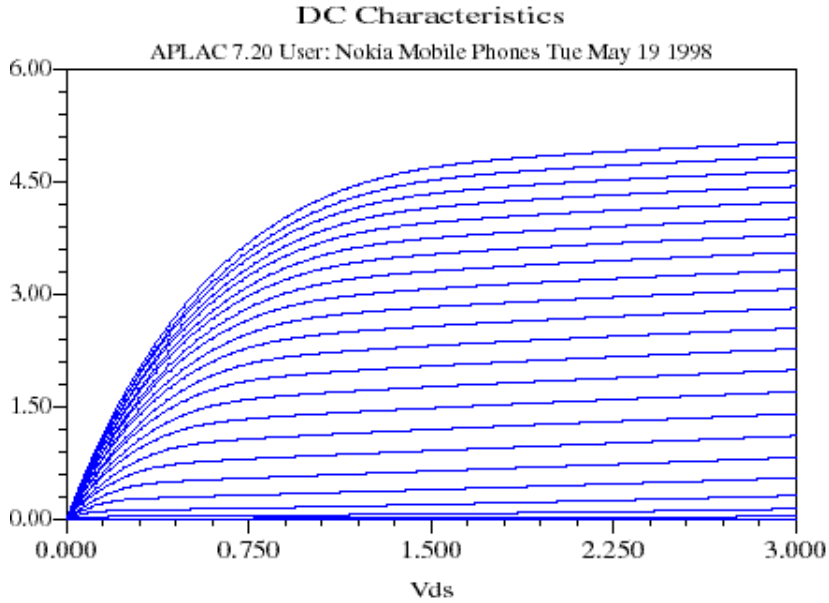

Figure 2.7 I-V characteristic of a typical submicron NMOS transistor.

The knee voltage is defined as the drain voltage at which the transistor starts operating in saturation for a given gate voltage. Due to the knee effect it is not possible obtain maximum voltage and current swing using the same load-line, actually maximum

voltage swing is only available at zero drain current. The impact of the knee effect can be calculated by realizing that only the values of V_{eff} and I_{eff} are affected. Since the value of I_{eff} affects only the output power of the power amplifier and V_{eff} affects output power as well as efficiency it is possible to make trade-offs between output power and efficiency for a given transistor.

To illustrate how seriously the knee-effect reduces the efficiency the output power and efficiency is plotted vs. knee-voltage in Figure 2.8 for a class B amplifier.

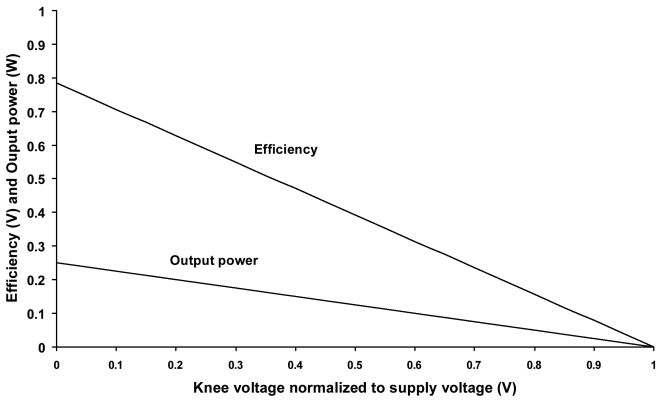

Figure 2.8 Efficiency and output power vs. knee-voltage for a class B amplifier.

Now that the general coverage of the classes A through C is done, it is natural to discuss the specific behavior of the original class definitions. This will be done in the following sections.

2.1.2 Class A

The conduction angle of a class A amplifier is $360°$. The maximal efficiency of a class A amplifier is therefore 50%. The class A amplifier is the class with the best linearity, but also the lowest efficiency. Ideally the load line of a class A amplifier is placed in such a way that the quiescent current is half that of the maximal current needed. The drain efficiency of a class A amplifier is given by [1][2]:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{I_q^2 \cdot R_L^2}{2 \cdot V_{dd}^2} \qquad \textbf{(2.17)}$$

The load which gives the maximum power at the output is V_{dd} / I_q, with this load the maximum efficiency is 50%. When the saturation voltage of the device is taken into account, the situation is even worse. The possible voltage swing is then only $V_{dd} - V_{knee}$, this gives the load line $(V_{dd} - V_{knee}) / I_q$. The maximum efficiency is then given by:

$$\eta_{max} = \frac{\left(1 - \frac{V_{knee}}{V_{dd}}\right)^2}{2} \quad \textbf{(2.18)}$$

For a 3.3 V process with a knee voltage of 0.5 V the maximum efficiency will be 42%. Although the efficiency is poor at maximum output power, it gets even worse when less than maximum power is needed since the DC power P_{DC} is unchanged, but the output power P_{out} is lower.

2.1.3 Class B

The class B amplifier is biased in such a way that it amplifies only the positive part of the signal. In the remaining part of the time, the output from the amplifier is zero. Since the conduction angle of a class B amplifier is only $180°$, a filter must be placed at the output in order to filter the harmonics out of the signal. Another way to retrieve the original signal is to couple two class B amplifiers in a push-pull configuration.

The class B amplifier is basically linear and has a maximum efficiency of 78.5% with $V_{knee} = 0$, this can be shown for a single-ended amplifier as below.

$$I_p = \frac{V_{dd} - V_{knee}}{R_L} \quad \textbf{(2.19)}$$

$$P_{out} = R_L \cdot \frac{1}{T}\int_0^{\frac{T}{2}} (I_p \sin\omega t)^2 d\omega = \frac{I_p^2 \cdot R_L}{4} = \frac{(V_{dd} - V_{knee})^2}{4 \cdot R_L} \quad \textbf{(2.20)}$$

$$P_{DC} = I_D V_{dd} = \frac{I_p V_{dd}}{\pi} = \frac{V_{dd} \cdot (V_{dd} - V_{knee})}{\pi \cdot R_L} \quad \textbf{(2.21)}$$

$$P_{diss} = \frac{1}{T}\int_0^T i_{DS}(t) v_{DS}(t) dt \quad \textbf{(2.22)}$$

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{(V_{dd} - V_{knee})^2}{4 \cdot R_L} \cdot \frac{\pi \cdot R_L}{V_{dd} \cdot (V_{dd} - V_{knee})} = \frac{V_{dd} - V_{knee}}{V_{dd}} \cdot \frac{\pi}{4} \quad \textbf{(2.23)}$$

2.1.4 Class AB

Class AB amplifiers are biased in such a way that the conduction angle is between $180°$ and $360°$. The maximal efficiency is therefore between 50% and 78.5% depending on the conduction angle. In practice most class B amplifiers will be designed slightly into the class AB region, due to the nonlinearities of the turn-on region in the transistor. This means that a vast majority of the power amplifiers for wireless communications operate in class AB.

2.1.5 Class C

In a class C amplifier the conduction angle, θ,is less than $180°$. The efficiency depends upon the conduction angle and can ideally reach 100%. As the efficiency rises the power gain decreases, and the power added efficiency, will eventually fall to 0. The Class C amplifier operates highly non-linearly.

$$P_{out} = \frac{I_p^2 \cdot R_L^2}{4\pi^2} \cdot (2\theta - \sin 2\theta)^2 \quad \textbf{(2.24)}$$

$$P_{DC} = \frac{V_{dd} \cdot I_p}{\pi} \cdot (\sin\theta - \theta\cos\theta) \quad \textbf{(2.25)}$$

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{2\theta - \sin 2\theta}{4(\sin\theta - \theta\cos\theta)} \quad \textbf{(2.26)}$$

2.2 Class D and F

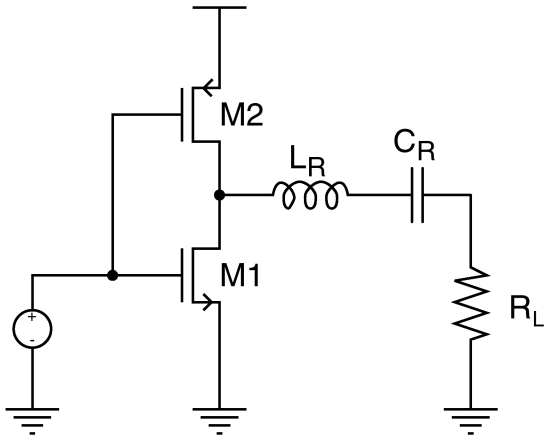

Figure 2.9 Class D amplifier.

Much like the class A-C power amplifiers it is possible to treat class D and F as special cases of the same general theory. The original definition of a class D power amplifier uses two transistors operated as switches, see Figure 2.9. The on-resistance and therefore the loss in the transistor should be zero. The efficiency is limited by the switching time and the on-resistance of the transistor. Due to the switching behavior of the class D amplifier it is very non-linear and in principle not even power control is possible. The drain efficiency of a class D power amplifier is given by [2]:

$$V_{eff} = V_{DD}\frac{R_{dc}}{R_{dc} + R_{on}}, R_{dc} = \frac{8R_L}{\pi^2} \quad \textbf{(2.27)}$$

$$\eta = \frac{V_{eff}}{V_{dd}}\frac{\sin\theta_s}{\theta_s} \quad \textbf{(2.28)}$$

where $\theta_s=2\pi t_s$ is the angle associated with the switching. The transient time t_s is the time required for one of the transistor to switch. This means that the switching of the power amplifier is completed within $2t_s$.

The basic idea of class F amplifiers is to reduce the power dissipated in the transistor by minimizing the voltage across the transistor at the time where the current through the transistor is largest. This is accomplished by modifying a class B amplifier with a quarter-wave stripline to short all even harmonics and appear as open at odd harmonics, while the fundamental does not see the load as normal. The harmonic termination means that the waveform of the output signal will be a square wave. This gives a maximum achievable efficiency of 100% and is actually the same condition as class D although single-ended [3].

Instead of a stripline a 3rd harmonic termination using a resonator consisting of an inductor and a capacitor can be used. The maximum achievable efficiency for this type of amplifier is then approximately 88%, which is about 10% better than the class B amplifiers. The principle of the class F power amplifier with third harmonic termination is shown in Figure 2.10.

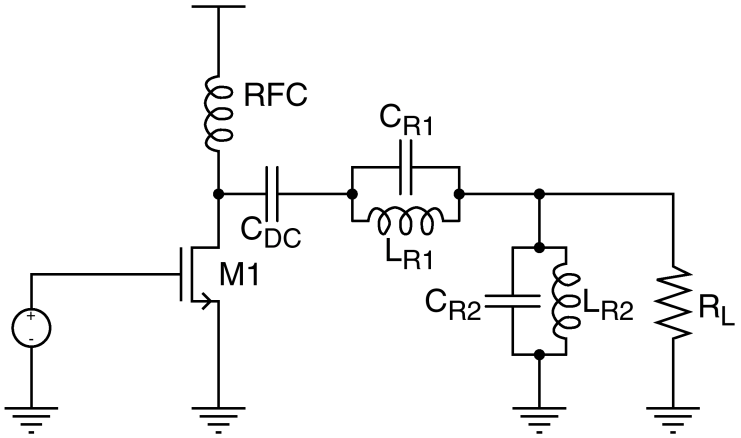

Figure 2.10 Class F power amplifier with third harmonic termination.

It is also possible to use a 2nd harmonic termination. The maximum achievable efficiency for this type of amplifier is then approximately 85%. A number different configurations are possible, but in general the increased efficiency is followed by increasing complexity. It is also important to bear in mind that the increased complexity increases the total losses in the nonideal passive components.

2.3 Class E

The class E amplifier is a tuned amplifier, which ideally can reach an efficiency of 100% [4]. The transistor works as a switch as is the case with class D amplifiers, but only one transistor is used. The basic idea is to delay the voltage curve so that the drain voltage does not rise till after the switching is done. This kind of operation causes the class E amplifier to be very nonlinear. Even for a non-ideal transistor the efficiency of a class E power amplifier can be quite high.

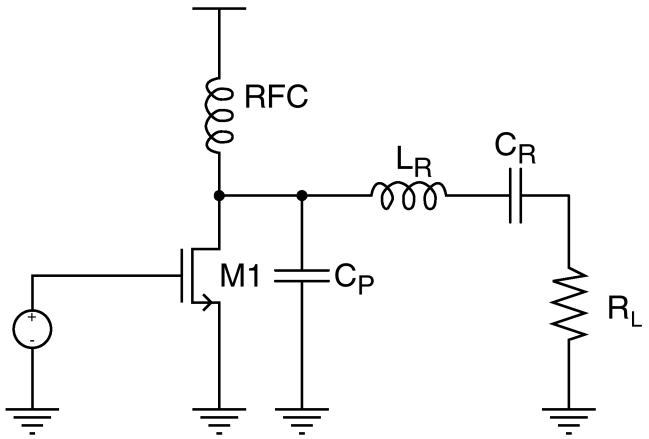

Figure 2.11 Generic class E power amplifier.

The design of a class E power amplifier is characterized by the choice of conduction angle, supply voltage and peak current. The output power and peak voltage depends on the conduction angle. This means that they both rise with increasing conduction angle. For a reasonable output power the peak voltage is at least three times the supply voltage. This causes problems if the transistors used have relatively low breakdown voltage.

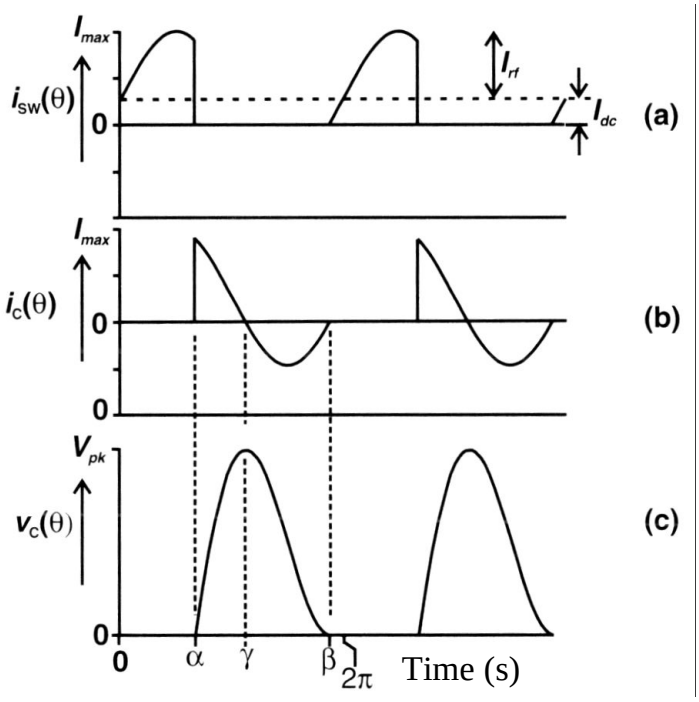

Figure 2.12 Drain and capacitor current and drain voltage of a class E PA [1].

2.4 Class S

The class S amplifiers operate in the same way as class D, but the pulse width is modulated. The class S amplifier demands even faster transistors than the class D

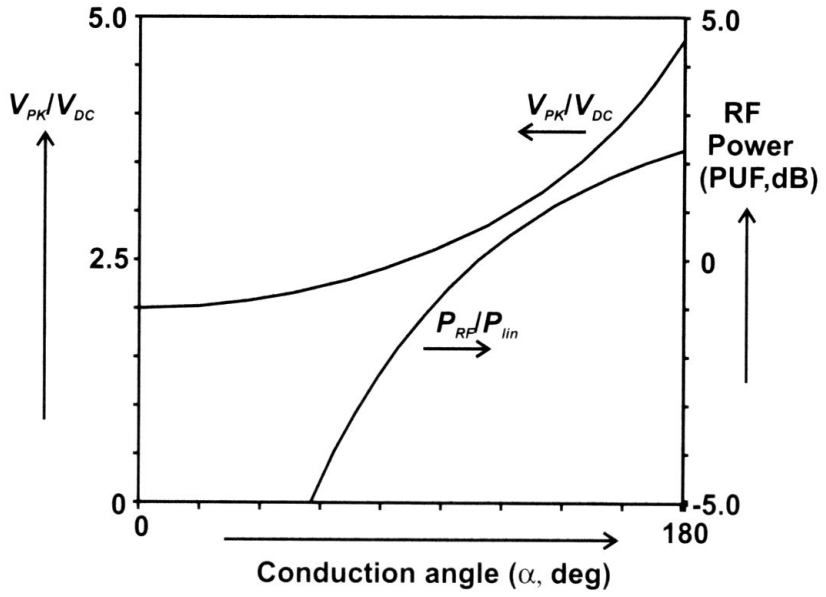

Figure 2.13 Output power and peak voltage vs. conduction angle [1].

amplifier, since the pulsewidth modulation causes very short pulses to be generated. Once again the efficiency can ideally reach 100%.

The pulsewidth modulations means that the power amplifier acts linearly assuming the pulsewidth modulation is linear. In principle this configuration makes it possible to build very high efficiency power amplifiers, but the generation of the pulsewidth modulation is very troublesome.

One approach to the pulsewidth modulation is ΣΔ-modulation [5], this is illustrated in Figure 2.14. The RF signal is then oversampled, e.g. an oversampling rate of eight. The drawback of this approach is that the digital logic will have to run at eight times the frequency of the RF signal. At these frequencies the digital logic will have a large power consumption which will degrade the total efficiency. Another drawback is the need for a bandpass filter at the output of the power amplifier.

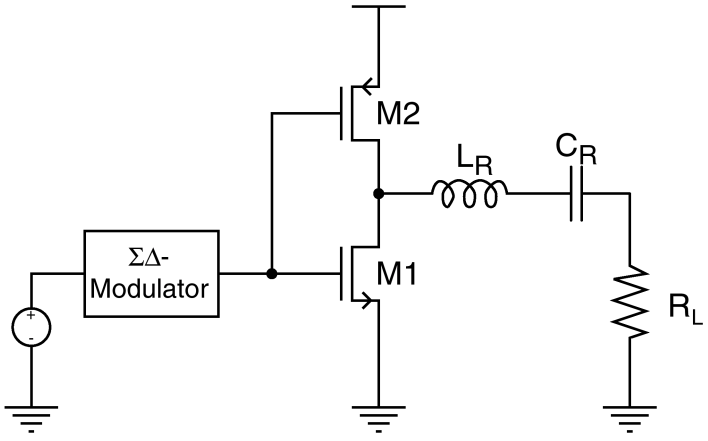

Figure 2.14 Class S power amplifier with ΣΔ-modulation.

2.5 Differential Power Amplifiers

The differential power amplifier differs from an ordinary power amplifier in a number of ways. There are advantages as well as disadvantages of differential power amplifiers. In principle a differential amplifier might just be two separate amplifiers coupled in parallel, although a lot of the advantages will not be available then.

One of the big challenges of high efficiency power amplifiers is the inductance in series with the ground. The effect of the ground inductance can be reduced by a differential amplifier.

One of the main motivations to use differential power amplifiers is the tempting idea that they can drive a differential antenna. The differential antennas have not yet proven to be usable in mobile phones. One of the problems with differential antennas is that the specific absorption rate (SAR) is higher than in single-ended antennas. Another problem with the differential antennas is the fact that either the efficiency or the bandwidth of the antennas drops when operated in differential mode. Since the bandwidth of an antenna for mobile phones is already close to the specifications, a differential antenna will have lower efficiency, thereby eliminating the best argument for differential power amplifiers.

If a differential power amplifier will have to drive a single-ended antenna a differential to single-ended conversion will have to take place somewhere after the power amplifier. A differential to single-ended conversion is always associated with loss and increased cost.

2.6 Summary

As described above there are numerous classes of operation, with different advantages and disadvantages. In order get a quick overview of the different classes Table 2.1 can be used.

Table 2.1 Quick overview of the classes of operation.

Class	Maximum efficiency	Linearity	Note
A	50%	Good	
AB	50-78.5%	Fair	
B	78.5%	Fair	
C	78.5-100%	Poor	
D	100%	Poor	
E	100%	Poor	
F	85%	Fair	2nd harm.
F	88%	Fair	3rd harm.
F	100%	Fair	Even harm.
S	100%	Good	

For a more detailed comparison, the properties of the transistor have to be included, especially the maximum power gain, the supply voltage and the knee voltage.

In practice only a few of the classes of operation are useful for wireless communication. The class A power amplifier is typically used for basestations as well as mobile phone standards with high linearity requirements. The class AB power amplifiers are used for a broad range of mobile phones. The class C power amplifiers are also in use but typically introduce practical problems due to the relatively low output power for a fixed transistor size.

The class B power amplifier does not exist in practical applications due to the nonideal devices, which will cause the power amplifier to operate in either class AB or C. The class D and E power amplifiers are difficult to use since they do not even facilitate power control, class S on the other hand is almost impossible to use at RF frequencies.

The only class of operation not in common use, which is suitable for wireless communications is the class F power amplifier. The class F power amplifier is currently the subject of a lot of research.

If one of the strongly nonlinear class of operation is to be used for wireless communications one of the linearization systems will have to be introduced, but in general they add complexity as well as lower the total efficiency.

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[5] M. Iwamoto, J. Hinrichs, J. Arun, L. Larson, and P. M. Asbeck, "A push-pull bandpass delta-sigma class-S amplifier," in *2000 IEEE Topical Workshop on Power Amplifiers for Wireless Communications Technical Digest*, September 2000.

CHAPTER 3

LOAD-LINE THEORY AND IMPEDANCE MATCHING NETWORKS

As explained in Chapter 2 the load impedance along with the class of operation are probably the most important aspects of power amplifier design. The source impedance of the power amplifier stage will of course also have to be selected.

In the following sections a number of methods for selecting the source and load impedances will be described. First the small-signal methods will be introduced, since they are simple and can be based on S-parameter data which are usually available. After the small-signal methods the large-signal methods will be described. The classical load-pull measurement technique will be introduced. Then a similar simulation technique will be developed for use in integrated circuit design.

After the proper source and load impedances has been selected, the impedance matching networks must be synthesized. The different kinds of matching networks will be described in this chapter. The steps involved in synthesis of the impedance matching networks will also be explained. The synthesis methods will also be used as a part of the load-pull simulation method.

3.1 Small-Signal Impedance Matching

The small-signal impedance matching approaches are primarily suited for small-signal RF components such as LNAs. It is however useful to know the small-signal impedance matching methods, since they can be used as a starting point for especially the matching of the input of the power amplifier. The small-signal impedance matching methods are all based on the properties of S-parameters which will be described shortly in the following section.

To obtain maximum gain in a device the transducer gain method is used. It is however not always desirable to achieve maximum gain match, since other parameters such as noise and output power might be more important than the gain of the amplifier. This means that the matching network is often a compromise between gain, output

power and noise. There are two methods to optimize the trade-offs of the matching networks, namely the operating gain method and the available gain method. All of the above mentioned matching methods will be described in the following sections.

3.1.1 S-Parameters

The scattering parameters, better known as S-parameters, is the most common set of small-signal parameters used to characterize RF devices, active or passive. This is due to the fact that Z and Y parameters can not be measured accurately at RF frequencies. The difficulties of measuring Z and Y parameters at RF frequencies are caused by the lack of good open and short terminations at RF frequencies. Furthermore the short-circuits used in Z and Y parameter measurements, will often cause the device under test (DUT) to become unstable.

The S-parameters are measured using normalized incident and reflected travelling waves of transmission lines at the ports. The four parameters of a two-port S-parameter measurement are:

S_{11} = the input reflection coefficient

S_{12} = the reverse transmission coefficient

S_{21} = the forward transmission coefficient

S_{22} = the output reflection coefficient

Once the S-parameters have been measured it is of course possible to convert them to other small-signal representations, e.g. Z and Y parameters.

3.1.2 The Smith Chart

The Smith chart is used to represent the S-parameter data described above. The Smith chart is a graphical representation of the reflection coefficient plane, the Γ plane, with the relation

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}, \qquad \mathrm{Re}[Z] \geq 0 \qquad \textbf{(3.1)}$$

where Z_0 is the reference impedance value. The basic Smith chart is shown in Figure 3.1. The advantage of the Smith chart is that it is possible to depict all impedances with a positive real part in a finite chart. The Smith chart is constructed of circles representing constant resistance and constant reactance.

Another feature of the Smith chart is the possibility to plot a number of important RF parameters as circles. Examples are stability circles, noise circles and constant Q circles[1][2][3].

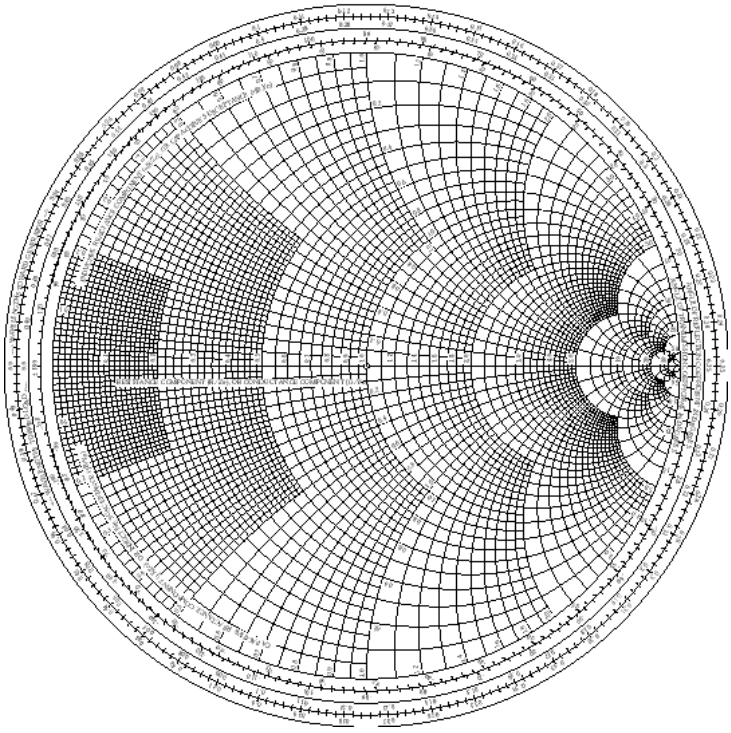

Figure 3.1 The Smith chart.

3.1.3 Transducer Gain Method

The maximum gain match condition is when no power is reflected at neither the input port nor the output port, this will give the maximum small-signal gain of the device. This maximum gain match is obtain by connecting a source with an impedance equal to the complex conjugate to the impedance at the input port and a load equal to complex conjugate to the impedance at the output port. This is called the transducer gain method and can be used to obtain the maximum small-signal gain of a device. Depending on the characteristics of the device, either the unilateral or bilateral method can be used.

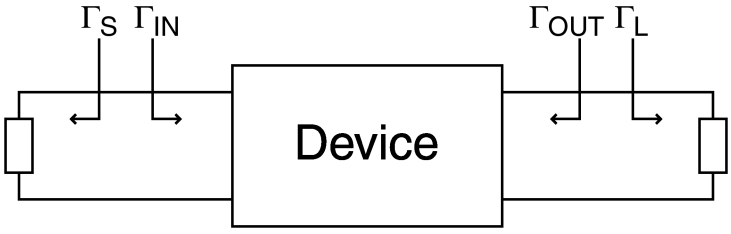

Figure 3.2 Definition of impedances used for matching a two-port.

The matching networks can be constructed by inductors, capacitors and striplines. The use of resistors is not optimal, since they will generate noise and dissipate power. The actual implementation of the matching networks will be described in Section 3.3.

The impedances at the input and output ports of the device can be written as [3][4]:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad \textbf{(3.2)}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad \textbf{(3.3)}$$

while the maximum gain achievable can be written as:

$$G_T = \frac{(1 - |\Gamma_S|^2)|S_{21}|^2(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_S\Gamma_L|^2} \quad \textbf{(3.4)}$$

The maximum stable gain can be found from:

$$G_{MSG} = \frac{|S_{21}|^2}{|S_{12}|^2} \quad \textbf{(3.5)}$$

Unilateral Method

As mentioned above the unilateral transducer gain method can be used to optimize the small-signal gain of a device. A two-port network is unilateral only if $S_{12} = 0$, that is when there is no reverse gain. Even though a transistor is not unilateral the method can still be used, but might not produce precise results. If it is assumed that $S_{12} = 0$, then (3.4) can be rewritten as:

$$G_{TU} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad \textbf{(3.6)}$$

It can be seen that the equation then consists of three terms. The first term depends only on the source reflection Γ_S and the input reflection of the device S_{11}. The second term depends only on the forward gain S_{21}. The last term depends on Γ_L and S_{22}. It is then obvious that the gain can be optimized by optimising the three terms separately. If the device is left unchanged only Γ_S and Γ_L is left. The optimal solution is then the case where $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$. The maximum gain is then:

$$G_{TU,\,max} = \frac{1}{1 - |S_{11}|^2}|S_{21}|^2\frac{1}{1 - |S_{22}|^2} \quad \textbf{(3.7)}$$

As mentioned above this expression is only accurate for a truly unilateral device, and should be used with care on real devices.

Simultaneous Conjugate Match

The simultaneous conjugate match method can be used when the device is not unilateral. The source and load terminations of the transistor can be derived from (3.4) [3]. The matched source reflection is:

$$\Gamma_{MS} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad \textbf{(3.8)}$$

where B_1 and C_1 are:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad \textbf{(3.9)}$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad \textbf{(3.10)}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad \textbf{(3.11)}$$

The matched load reflections is:

$$\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad \textbf{(3.12)}$$

and B_2 and C_2 are:

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad \textbf{(3.13)}$$

$$C_2 = S_{22} - \Delta S_{11}^* \quad \textbf{(3.14)}$$

3.1.4 Available Gain Method

The available gain method is used when the matching of the input port is the most important as is the case for applications such as low noise amplifiers as well as the input stage of a multistage power amplifier. The source impedance can be chosen arbitrarily and the output of the device can then be conjugately matched [3][5].

$$G_A = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_{OUT}|^2} \quad \textbf{(3.15)}$$

Equation (3.15) can be used to find the maximum gain for the given source impedance, but to be able to make the trade-offs usually involved in RF design it can be useful to have constant gain circles instead. The constant gain circles will indicate where the gain has dropped by a certain amount, e.g. 1 dB. Combined with for instance the noise circles often used in LNA design, it is possible to make a trade-off between gain and noise. The output impedance associated with the center of the gain circle is:

$$G_A = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1}{1 - \left|\frac{S_{22} - \Delta\Gamma_S}{1 - S_{11}\Gamma_S}\right|^2} \quad \textbf{(3.16)}$$

$$g_A = \frac{G_A}{|S_{21}|^2} \quad \textbf{(3.17)}$$

$$C_A = \frac{g_A C_1^*}{1 + g_A(|S_{11}|^2 - |\Delta|^2)} \quad \textbf{(3.18)}$$

The radius of a gain circles is determined by:

$$r_A = \frac{\sqrt{1 - 2K|S_{12}S_{21}|g_A + |S_{12}S_{21}|^2 g_A}}{\left|1 + g_A(|S_{11}|^2 - |\Delta|^2)\right|} \qquad \textbf{(3.19)}$$

In Figure 3.3 a typical set of constant gain circles are shown. The circles shown represent the impedances where the gain has dropped 1, 2 and 3dB respectively.

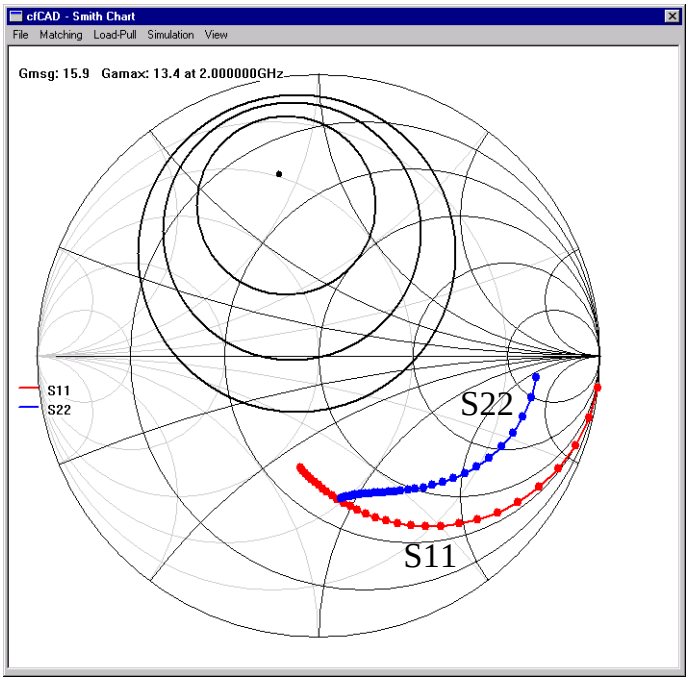

Figure 3.3 Constant gain circles associated with the available gain method.

3.1.5 Operating Gain Method

When the selection of the load impedance is the most important parameter, as is the case with power amplifiers, the operating gain method is used. Using the operating gain method, the load impedance is arbitrarily defined, and the source is then matched. The power gain can then be calculated as [3][6]:

$$G_P = \frac{1}{1-|\Gamma_{IN}|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad \textbf{(3.20)}$$

In (3.20) the input impedance is replaced by (3.2) giving

$$G_P = \frac{1}{1-\left|\frac{S_{11}-\Delta\Gamma_L}{1-S_{22}\Gamma_L}\right|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad \textbf{(3.21)}$$

Since the operating gain method is good when the load impedance is already chosen this will often be the small-signal matching method of choice when the source impedance of a power amplifier is selected. As was the case with the available gain

method it is possible to draw gain circles based on the chosen load impedance. To simplify the equations it is useful to define the variable g_p:

$$g_P = \frac{G_P}{|S_{21}|^2} \tag{3.22}$$

The center of a given gain circle is given by:

$$C_P = \frac{g_P C_2^*}{1 + g_P(|S_{22}|^2 - |\Delta|^2)} \tag{3.23}$$

where C_2 is defined as:

$$C_2 = S_{22} - \Delta S_{11}^* \tag{3.24}$$

As was the case for the available gain method it can be useful to plot gain circles. The radius of the gain circle calculated by:

$$r_P = \frac{\sqrt{1 - 2K|S_{12}S_{21}|g_P + |S_{12}S_{21}|^2 g_P^2}}{|1 + g_P(|S_{22}|^2 - |\Delta|^2)|} \tag{3.25}$$

In Figure 3.4 a typical set of constant gain circles are shown. If the device is conditionally unstable part of the gain circles will be placed outside the Smith chart. The $G_{P,max}$ can then be replaced by the maximum stable gain G_{MSG}, an example of the gain circles of a conditionally unstable device is shown in Figure 3.5. As can be seen in the figure the gain circles intersect the Smith Chart in the same points as the stability circles.

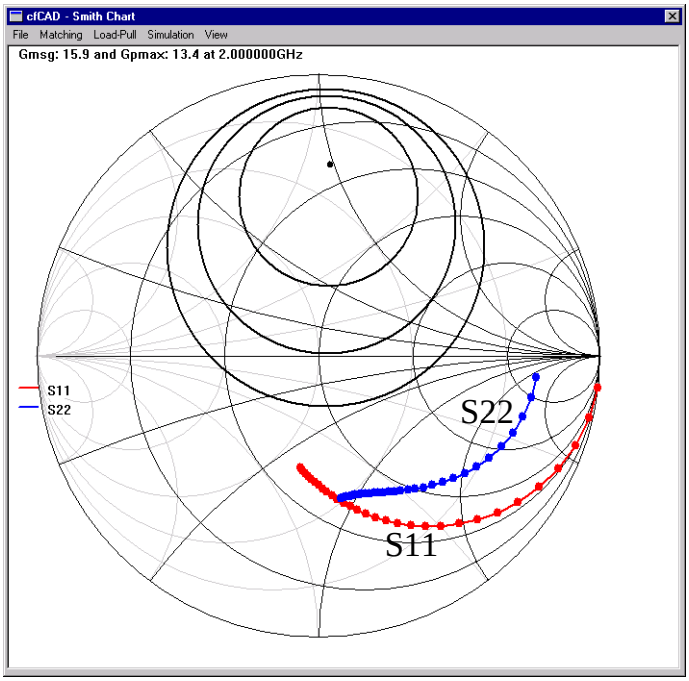

Figure 3.4 Constant gain circles associated with the operating gain method.

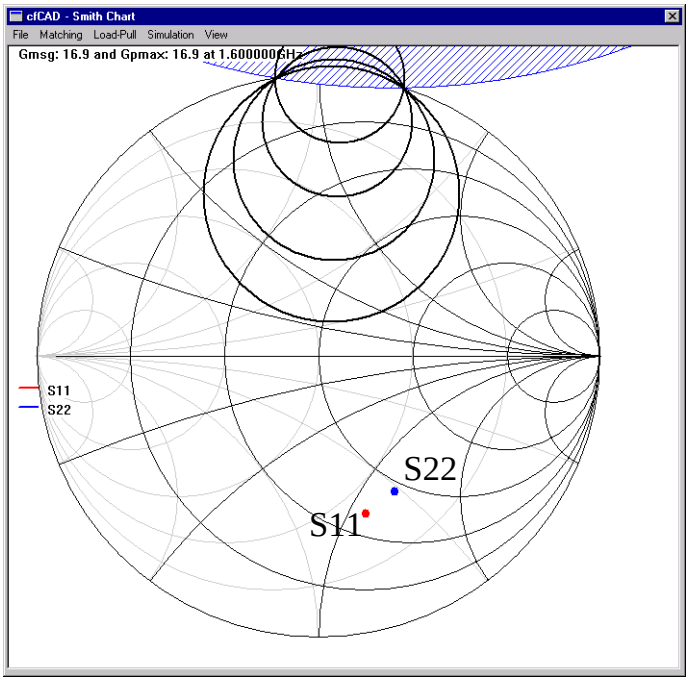

Figure 3.5 Operating gain circles of a conditionally unstable device.

3.2 Large-Signal Impedance Matching

All of the methods described above are based on the small-signal behavior of the device, but in a power amplifier the device is usually driven far into the nonlinear region of operation. One way to take the large-signal model into account is the load-pull method.

3.2.1 Load-Pull Contours

Load-pull contours represents the behavior of a given parameter as a function of the load impedance as was the case with e.g. the gain circles in the small-signal approaches. Load-pull contours can be created using measurements, simulations or analytical approaches. In the measured and simulated load-pull methods the load is varied systematically while the source impedance is kept at a fixed impedance or continuously kept conjugate matched according to the small-signal matching theory. This can be performed with either measurements on a real device or within a large-signal simulator.

The analytical approach to load-pull was introduced by S. Cripps in 1983 [7]. The starting point in this approach is the ideal load-line theory, and the transistor is thought of as an ideal current source with lumped parasitic elements. The basic idea is then to identify which impedances will give e.g. the 1 dB contour. It is however cumbersome to de-embed the intrinsic transistor and measured or simulated load-pulling will usually be preferred. Furthermore it is virtually impossible to define a linear drain-source capacitance in e.g. submicron CMOS, since this capacitance is very nonlinear.

One of the most common parameters plotted as a load-pull contour is the output power at the 1dB compression point. When the simulations or measurements have been performed the contours are found, e.g. the contour where the output power has dropped 1dB compared to the maximum achievable output power. An example of this plot is shown in Figure 3.6, where the 1, 2 and 3dB output power contours are shown. Unfortunately the large-signal contours are not circles as is the case for most small-signal parameters. The large-signal contours can therefore not be manipulated as easily as e.g. the small-signal gain circles.

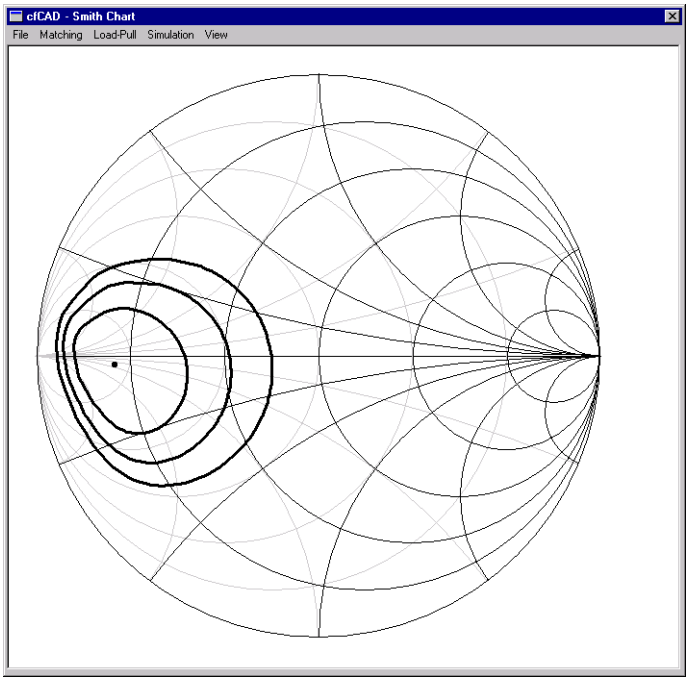

Figure 3.6 1,2 and 3dB output power contours.

The output power at 1dB compression point is not the only interesting parameter that can be found using load-pulling, other parameters that can be found are power added efficiency and various distortion parameters. In practice all parameters of a power amplifier that are measured or simulated to characterize a power amplifier can be used in a load-pull analysis. Combining different types of contours gives the designer the opportunity to make trade-offs based on the results. One of the most common trade-offs is the one between output power and power added efficiency, the combination of output power and power added efficiency contours is shown in Figure 3.7. The power added efficiency contours are plotted in 5% steps relative to the maximum efficiency, while the output power contours are in 1dB steps.

3.2.2 Load-Pull Measurement Systems

A basic load-pull measurement system is shown in Figure 3.8 [8]. Since a very large number of measurements will have to be made, a computer is used to control the measurement equipment. The heart of the system is a tuner placed at the output of the power amplifier. The tuner transforms the load on its output from the standard 50Ω load to any given impedance at the input of the tuner. Since there are parasitics between the

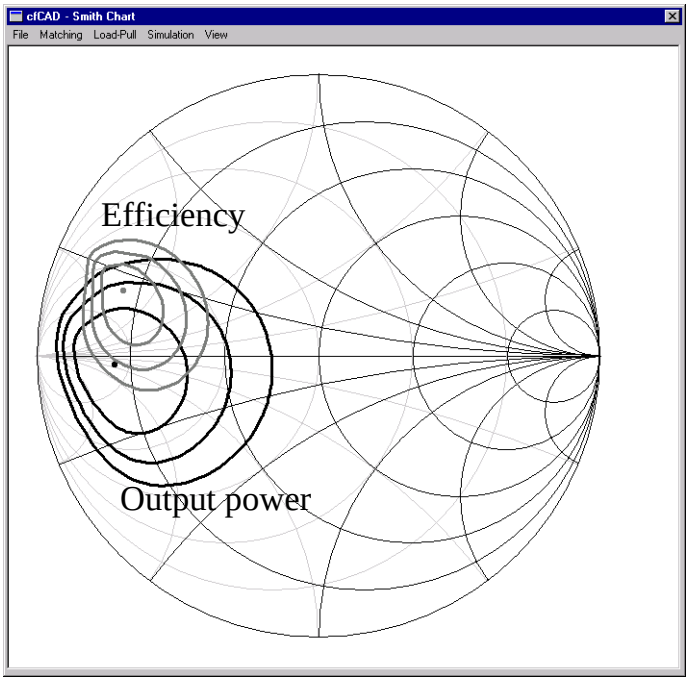

Figure 3.7 Trade-off between output power (black) and power added efficiency (grey).

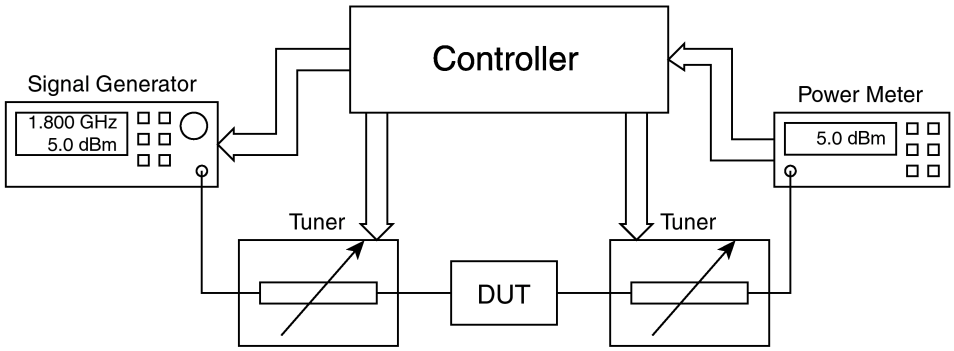

Figure 3.8 Basic Load-Pull System [8].

output of the power amplifier and the input of the tuner as well as some internal parasitics the are some limitations to which impedances can be generated at the output of the power amplifier.

The tuner can be implemented mechanically as for instance a sliding stub. The stub can then be moved using a stepping motor. An important aspect when doing load-pull measurements is the repeatability of the equipment, this means that the tuners should reproduce exactly the same impedance every time they are used. If the repeatability is not good the calibration performed before the actual measurements is without value.

To avoid the problems with repeatability in mechanical tuners it is possible to implement electromechanical tuners using pin-diodes. This gives high repeatability and switching speed, but the insertion loss is higher than in the purely mechanical tuner.

At last it is possible to use active tuners. The active tuners uses an auxiliary power amplifier and a phase shifter to generate a virtual load impedance.

In the basic load-pull system only the fundamental frequency is tuned, but in more complex systems it is possible to gain control of the impedances at a number of harmonic frequencies. Since the measurements are done at discrete impedance points it is important to choose these carefully. Often the impedance points are chosen such that they give a uniform distribution in the Smith chart. It is seldom useful to get load-pull data outside a specified impedance range, since only data a couple of dBs below maximum gain are usable. In Figure 3.9 a typical set of load-pull impedance points are shown.

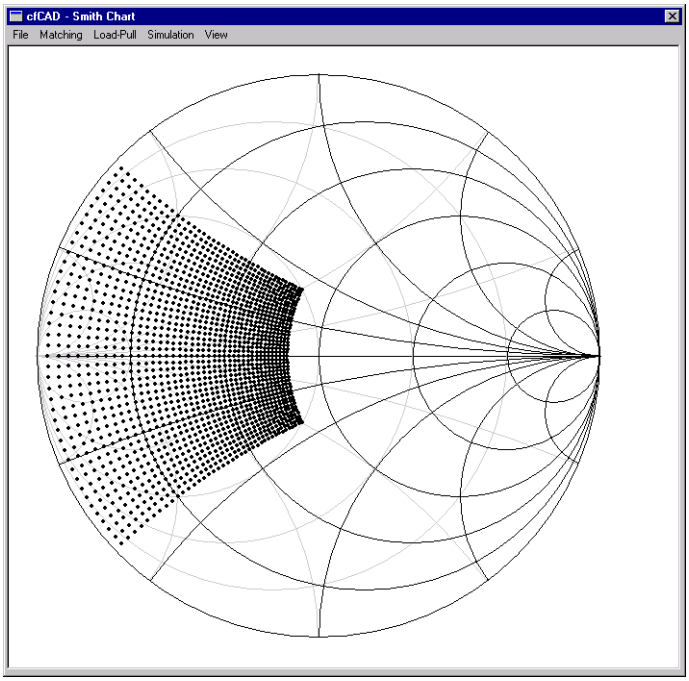

Figure 3.9 Impedance points chosen for load-pull measurements

The input of the power amplifier is typically matched using one of the small-signal methods or a fixed impedance point found experimentally. A signal generator is used to generate the input signal. At the output a vector signal analyzer or power meter is connected to the output of the tuner, to measure the desired parameters as a function of the varying load impedance.

Once the tuner has been setup for the correct load impedance, the wanted measurements can be performed. After the measurements have been performed the tuner is moved to the next impedance point. Once all the impedance points have been visited the computer will start postprocessing the data, this will then eventually result in the load-pull contours mentioned in Section 3.2.1.

3.2.3 Simulated Load-Pull

The simulated load-pull method is related to the measured load-pull, but with the important distinction that it is possible to use the simulated results during the design phase. Instead of using the tuners and measurements the simulated load-pull will use impedance matching networks and large-signal simulations. The large-signal simulation

can be either transient or steady-state, but the steady-state simulations will usually be preferred for minimum simulation time. In place of the tuner an impedance transforming network is used.

The wanted parameters, such as the output power and the efficiency, are then extracted for each value of the load. When doing load-pull simulations it is important to model the output device very carefully including the package.

The impedance used in the load-pull simulations can be realized in different ways. The first and simplest way is to use a series or parallel combination of ideal resistive and reactive components as shown in Figure 3.10.

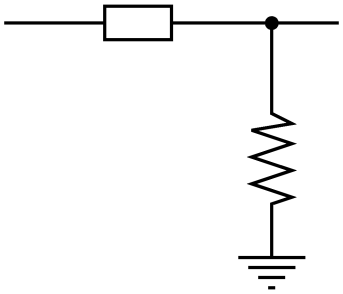

Figure 3.10 Load-pull impedance realized as a series combination.

Another and perhaps more realistic way to implement the impedance is to select the desired matching network topology and then calculate the necessary components values for the desired impedance. The synthesis of the topology and values of the components is the same as for the final networks and will be treated in the following sections. This approach is shown in Figure 3.11.

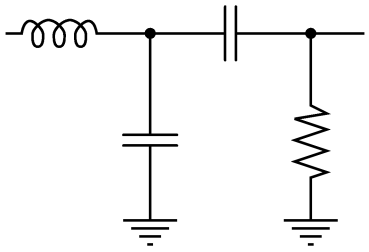

Figure 3.11 Load-pull impedance realized as a matching network.

The advantage of the last approach is especially that the frequency dependence of the matching network is built into the load-pull characteristics. This includes the impedances at the harmonic frequencies, which will have an influence on the efficiency, output power and distortion.

When the implementation of the load-pull impedance has been chosen, the simulation is carried out. The wanted parameters will be simulated at each impedance point selected. As was the case with measured load-pull the computer will postprocess the data generated and derive the load-pull contours.

3.3 Synthesizing Impedance Matching Networks

When the source and load impedances have been chosen it is necessary to synthesize the impedance matching network. This can be done using the Smith chart [3] or an analytical method [9]. Both approaches have been integrated in CAD tools.

When designing impedance matching networks inductors, capacitances and striplines are used almost exclusively, since resistive components are lossy. For size critical applications such as mobile phones the striplines are not very well suited due to their relatively large physical size.

The Smith chart is very useful, when designing impedance matching networks. The effect of a component is drawn as described in Section 3.3.2. The synthesis of the matching networks will be described for the graphical approach using the Smith chart as well as the analytical approach suitable for CAD tools. The synthesis of the matching networks are all based on alternating between series and parallel representation of the impedances.

The synthesis will only be explained for ideal components without parasitic effects. This is necessary to be able to keep the focus when designing the networks. Once the topology has been selected and the values of the components chosen it is easy to use a CAD tool to optimize the network to take the parasitic effects into account.

The bandwidth of a matching network is determined by the quality factor (Q) of the network. It might therefore be important to choose a matching topology that allows selection of the Q of the network. The Π and T matching sections allows increases in the Q, while cascading matching section allows reduction of the Q. All of these methods are described in the following sections.

3.3.1 Impedance Matching Basics

A complex impedance can be represented in either series or parallel form. This duality is actually the basis of the impedance matching methods described in the following. An impedance of $R+jX$ can be represented in either parallel or series form as illustrated in Figure 3.12.

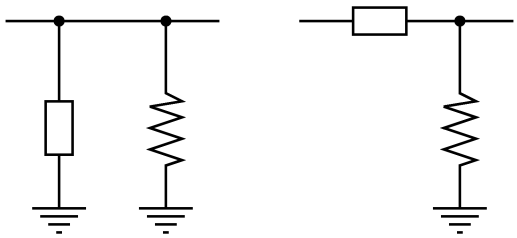

Figure 3.12 Series and parallel representation of a complex impedance.

This relation is used when synthesizing the impedance matching network. The network is synthesized by alternating between series and parallel impedance representation. In practice this done by adding series and shunt components.

The complex impedances are handled by modifying the component closest to the complex impedance. The basic principle in the handling of complex impedances is absorption of the reactive part of the impedance.

If the component closest to the load or source is a series component the load or source impedance will be represented by a resistor and a reactive part in series. If on the other hand the component is a shunt component the parallel representation of the impedance will be used.

3.3.2 Plotting Passive Components in the Smith Chart

As mentioned earlier the Smith chart is a very powerful graphically based tool, for RF designs. Although the Smith chart is graphically based, it is possible to use it as a tool for accurate impedance matching, especially when implemented in a CAD tool.

Usually only inductors or capacitors are used for impedance matching, and these may be added as either series or shunt components. The series components follow the constant resistance circles, while the shunt components follow the constant conductance circles. The traces in the Smith chart caused by the components are shown in Figure 3.13.

It can also be useful to use striplines as part of the matching networks, but depending on the use of the power amplifier it may be to area consuming on the PCB. The striplines will follow circles with a center equal to the center of the Smith chart.

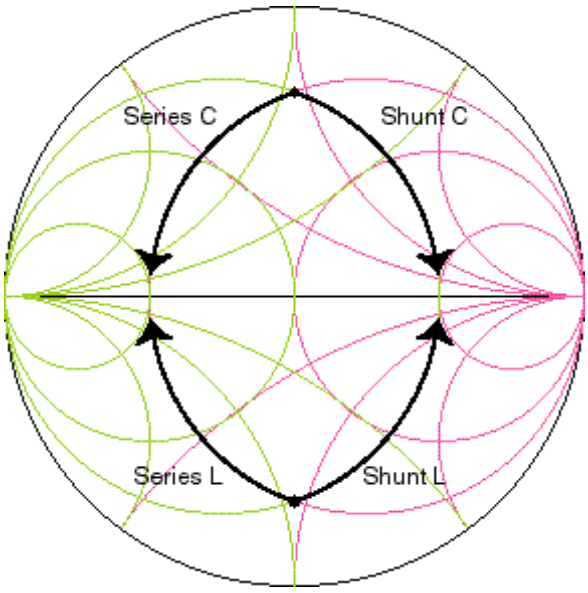

Figure 3.13 The effects of passive components plotted in the Smith chart.

3.3.3 The L Matching Section

Even though it is possible to design a large number of complex networks the simple L sections turns out to be quite useful. The L sections, see Figure 3.14, are all the possible combinations of a series and a shunt component. The frequency response of an L section can be classified as either a low-pass or a high-pass filter. If the transformation and the

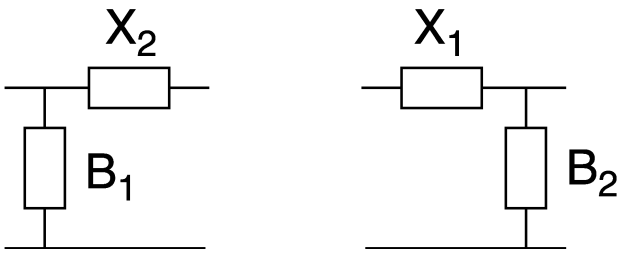

Figure 3.14 The L section matching networks.

frequency is determined for an L section, it is not possible to choose the transformation Q of the section.

The L sections will either increase or decrease the resistive part of the impedance depending on whether the first component is a series or shunt component. If the first component is a shunt component the transformation will decrease the impedance. If however the first component is a series component the impedance will be increased.

Since an L section with two capacitors or two inductors is not able to transform one purely resistive impedance to another only a limited number of L sections are left for general purpose transformations. For the general upward transformations two options are therefore available, namely series C-shunt L and series L-shunt C. In the case of downward transformation the options are shunt L-series C and shunt C-series L. These cases are easily synthesized for arbitrary source and load impedances.

An example of an L matching network is illustrated in the Smith chart in Figure 3.15. The figure is generated by a CAD tool using the methods described here. The impedance *10 - j10* should be matched to *50 + j20*. In this example a low-pass network has been selected and since the transformation is upward the network must be a Series L-Shunt C network. The intermediate impedance in the matching network can be found as:

$$Q = \sqrt{\mathrm{Re}(Z_{IN})\mathrm{Re}(Y_{OUT}) - 1} \qquad \textbf{(3.26)}$$

$$Z_B = \mathrm{Re}(Z_{IN})Q + j\frac{1}{\mathrm{Re}(Y_{IN})Q} \qquad \textbf{(3.27)}$$

$$X_L = \mathrm{Im}(Z_B) + \mathrm{Im}(Z_{IN}) \qquad \textbf{(3.28)}$$

$$B_C = \mathrm{Im}(Y_{OUT}) + \mathrm{Im}(Y_B) \qquad \textbf{(3.29)}$$

$$L_{series} = \frac{X_L}{\omega} \qquad \textbf{(3.30)}$$

$$C_{shunt} = \frac{1}{B_C\omega} \qquad \textbf{(3.31)}$$

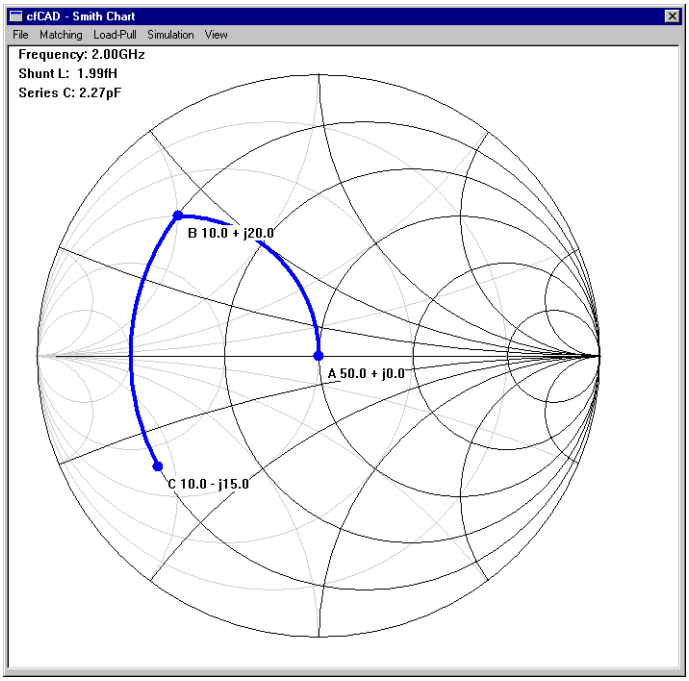

Figure 3.15 L matching network synthesized using CAD tool.

3.3.4 The T Matching Section

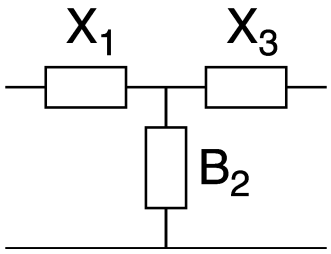

Figure 3.16 A Tee section.

A T section consists of a series component, a shunt component and then another series component. The T section actually contains two transformations. As was discussed in the section about L sections the transformation is upwards when the first component is a series component, then the shunt component transforms the impedance downwards while the last series component compensates the reactive part of the impedance.

Compared to the L sections, this gives the additional freedom of specifying the transformation Q of the matching network. When the T section is synthesized the Q of an equivalent L section can be used as a starting point to set the lower bound on the smallest transformation Q. If the transformation is upwards the first transformation Q is the highest. If the transformation is downwards the second transformation Q is the highest. It is not possible to reduce the highest transformation Q below the total transformation Q with a T section.

An example of a T matching network is illustrated in the Smith chart in Figure 3.17. The highest transformation Q is set to 5. The network is synthesized by finding the

series component that will intersect the Q circle. The intersection impedance as the input to an L section. The Q of an impedance point is given by the imaginary part of the impedance divided by the real part.

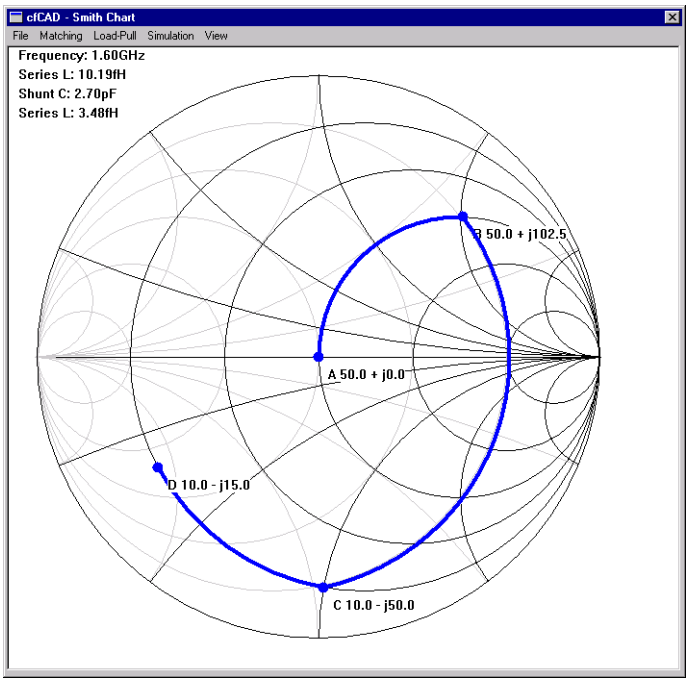

Figure 3.17 T matching network.

3.3.5 The Π Matching Section

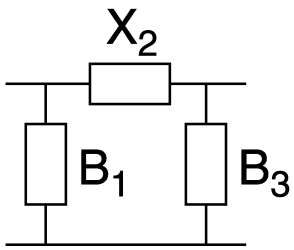

Figure 3.18 A Π section.

A Π section consists of a shunt component, a series component and then another shunt component. As was the case for T sections, the Π sections allows for the specification of the Q of the matching network.

As was the case with the T section the synthesis can be divided into two parts. The first part is to find the component that will give the highest Q. When the transformation is upwards the highest Q is in the second transformation. Again it is not possible for the highest transformation Q to be lower than for the L section. An example of a Π matching network is illustrated in the Smith chart in Figure 3.19.

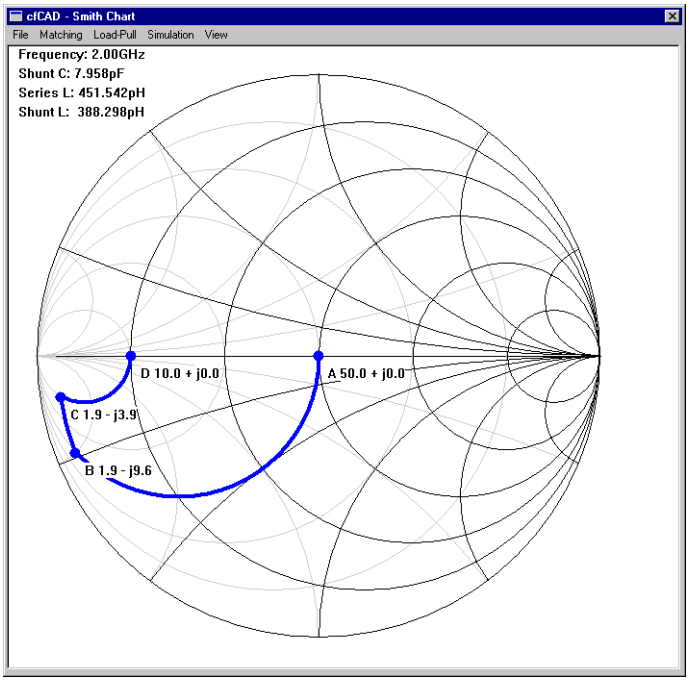

Figure 3.19 Π matching network.

3.3.6 Cascaded Matching Networks

If the transformation Q of a matching network is too high to sustain the bandwidth needed it is possible to cascade two or more of the above mentioned basic matching networks. For instance going from 1Ω to 50Ω would require a transformation Q of 7, if however two sections were cascaded the required Q of each section would be reduced to 2.5. In Figure 3.20 two cascaded L sections are illustrated. The impact on the bandwidth has been shown in Figure 3.21 where insertion loss of the two different circuits has been simulated. The 3dB bandwidth is in this example increased from 560MHz to 1060MHz.

It is of course necessary to take the loss in the nonideal components into account when deciding on the number of cascaded sections, since too many components may increase the losses of the components above the loss due to the Q of the matching network. The synthesis methods described here have all been implemented in the same software program as the load-pull simulation framework. This enabled the use of load-pull simulations using a more realistic impedance matching network.

3.4 Summary

The basics of impedance matching have been covered and small-signal as well as large-signal impedance matching methods have been described.

Since no tools were readily available for simulated load-pulling a software program was developed which will generate the input data to a large-signal simulator as well as process the output from the simulator to give the load-pull contours. The program

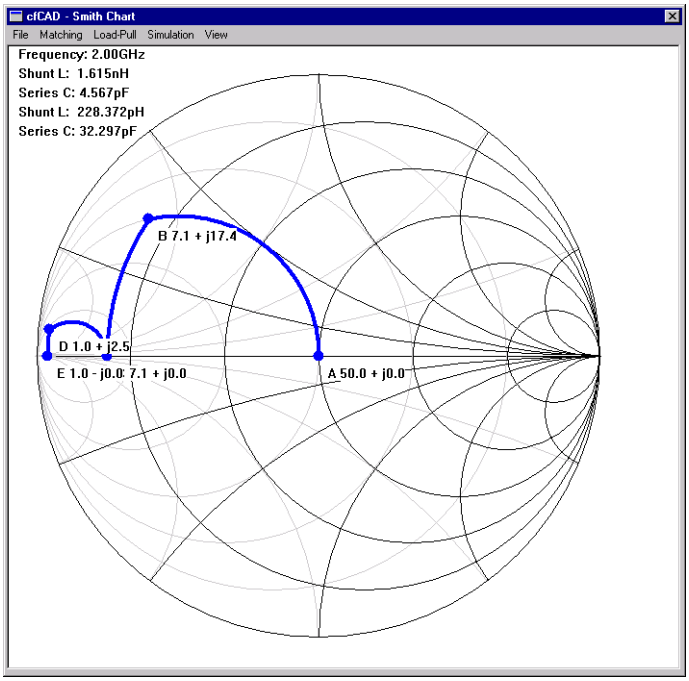

Figure 3.20 Two cascaded L sections.

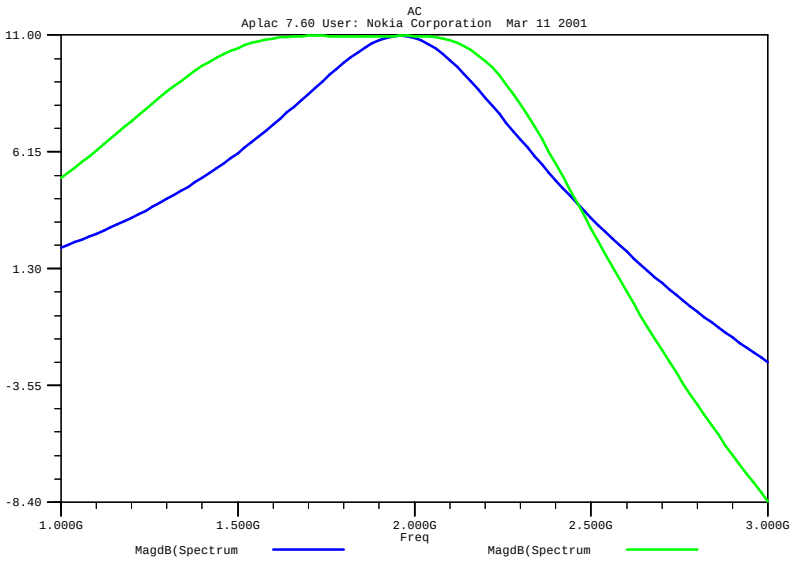

Figure 3.21 Insertion loss of one or two cascaded L section.

generates all information needed by the simulator and postprocesses the output data from the simulator thereby generating the output power and efficiency contours.

Furthermore the synthesis of the impedance matching networks has been described. The synthesis is generic and handles purely resistive as well as complex termination impedances. The synthesis of impedance matching networks with complex terminations has been presented with a combination of graphical and analytical aids.

The synthesis of impedance matching networks was used in conjunction with the load-pull simulations. The simulated load-pull method proves to a very powerful tool during the design phase. This is due to the immediate retrieval of measures of the

optimized performance of the circuit. Using the simulated load-pull method it is possible to use the obtain contours to make the necessary trade-offs between output power and efficiency. When these results are available in the design phase it is possible to optimize the circuit in an iterative process.

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CHAPTER 4
STABILITY AND BIASING

After choosing the class of operation and the impedance matching networks the basic behavior of the power amplifier has been determined. Two important issues which will also have to be taken into account when designing the matching networks are stability and biasing. Although these two topics do not directly affect properties like the efficiency of the power amplifier, they might cause the power amplifier to fail.

In the first part of this chapter the biasing of the power amplifier will be discussed. The biasing networks are discussed first since they influence the matching networks as well as the stability of the power amplifier.

In the remaining part of this chapter the stability of power amplifiers will be discussed as well as some measures to improve the stability of the power amplifier. The stability problems in a power amplifier can be divided into two types. The first problem is in-band oscillation caused by an unstable transistor. The second problem is instability caused by the biasing networks.

4.1 Bias Circuits

The biasing of the device is an important issue, since incorrect biasing may result in unstable or dysfunctional circuits. In order to minimize the effect of the biasing network, it has to be considered already when designing the matching networks. Some topologies for the matching networks can be used for biasing without modifications.

The biasing of CMOS transistors is usually easier than of bipolar transistors, since no DC power is consumed at the input.

4.1.1 DC Isolation

The input and output of a power amplifier is usually AC coupled, in order to get rid of the DC components. The DC isolation makes the biasing of the transistor much easier, since it is possible to set the input of the transistor to a specific DC value, without regard to the DC level of the input signal.

For a class B amplifier the input of the transistor will be DC biased exactly at the cut-off point. The DC isolation can be obtained with a series capacitor. The series capacitor will prevent a DC current to flow through it, but depending on the size of the capacitor an RF signal will flow unrestricted. It is then possible to apply a DC voltage after the capacitor to control the operation of the transistor.

4.1.2 RF Isolation

When applying the DC voltage as described above it is important to have good RF isolation, in order to keep the full input signal swing. This can be done with a series inductor which will allow a DC current to flow, but will restrict the RF signal depending on the size of the inductor. It is also possible to use a microstrip for the purpose of RF isolation, especially the quarter wavelength microstrip is useful. An example of a bias circuit for a MOSFET power amplifier using the DC and RF isolation techniques is shown in Figure 4.1.

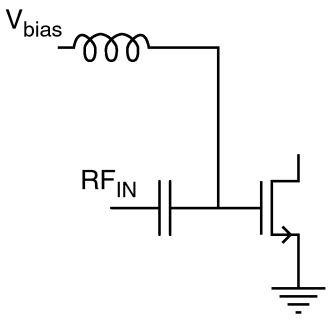


Figure 4.1 Bias circuit for MOSFET power amplifier.

4.1.3 Generating the Bias Signals

The DC signals can be applied directly from external signals or generated in the circuits based on an external signal. The DC signals will often be used dynamically for e.g. power control. When the bias signals are generated on-chip they can be purely passive circuits or active circuits which for instance provide temperature compensation. Examples of passive as well as active bias circuits are illustrated in Figure 4.2.

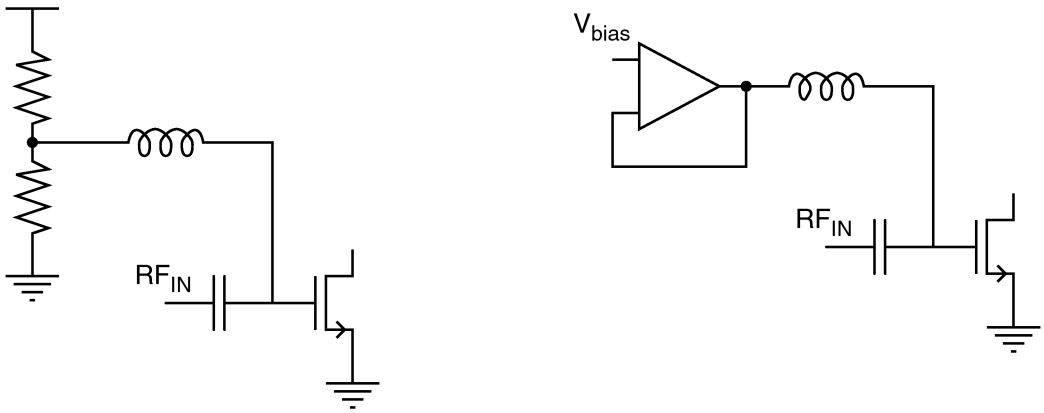


Figure 4.2 Passive and active bias circuit.

4.2 Stability of Power Amplifiers

A device can be characterized as either conditionally unstable or unconditionally stable. An unconditionally stable device is stable no matter what passive source and load impedances are connected to the ports of the device. A conditionally unstable device does not fulfil this requirement, and might start oscillating under certain conditions [1][2].

It is therefore important to analyze the stability of a device before using it in a power amplifier. Although the device might be stable with the nominal source and load impedances, these might change due to a shift in temperature, supply voltage or antenna shielding. It is therefore necessary to characterize the device under all realistic operating conditions.

4.2.1 Stability Circles

One way of visualizing the stability of the power amplifier is through stability circles. The conditionally unstable regions of the source and load impedances can be represented by stability circles in a Smith chart. The stability circle for the source impedance is given by the center and a radius [2]:

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \quad \textbf{(4.1)}$$

$$r_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \quad \textbf{(4.2)}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad \textbf{(4.3)}$$

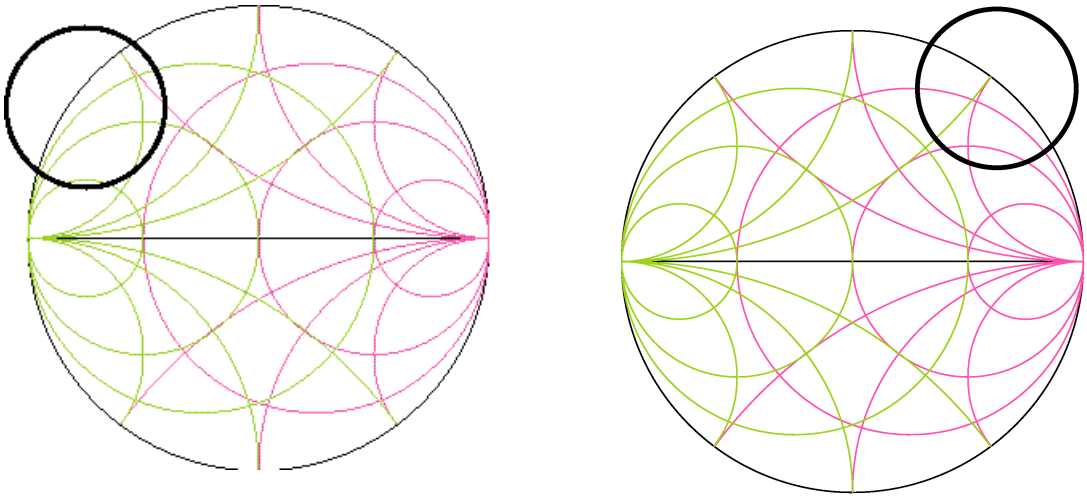
The center is a coordinate to be plotted in the Smith chart while the radius defines the contour. Whether the inside or the outside area of the circle is the stable region, has to be determined. This check can be performed by checking the stability of a single point. The stability circle for the load can be found equivalently:

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \quad \textbf{(4.4)}$$

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \quad \textbf{(4.5)}$$

Since the stability circles are calculated using S-parameters it is obvious that they depend upon the frequency. To assure that the device is stable over the entire frequency range, it is therefore necessary to plot the stability circles at a number of frequency points. Typical stability circles for a device is shown in Figure 4.3.

The device can be stabilized in a number of ways as described below, after the stabilisation it is then useful to extract new S-parameters for the stabilized device.

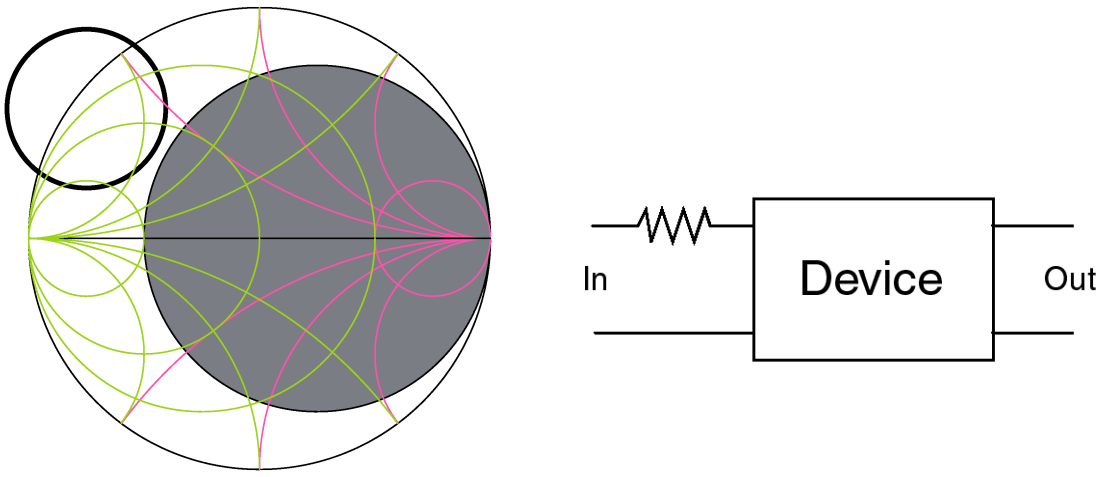


a) Typical source stability circle. **b)** Typical load stability circle.

Figure 4.3 Stability circles.

4.2.2 Resistive Stabilisation

One of the ways to stabilize a device is resistive stabilisation, this is usually at the input of the device, by connecting a resistor in series with the device. The input of the resistor is then considered to be the input port of the device. In this way it will never be possible to obtain an effective resistance lower than that of the resistor, and the conditionally unstable region can therefore not be reached. The resistive stabilization is shown in Figure 4.4, where the input impedance is then restricted to the grey area in the Smith chart.

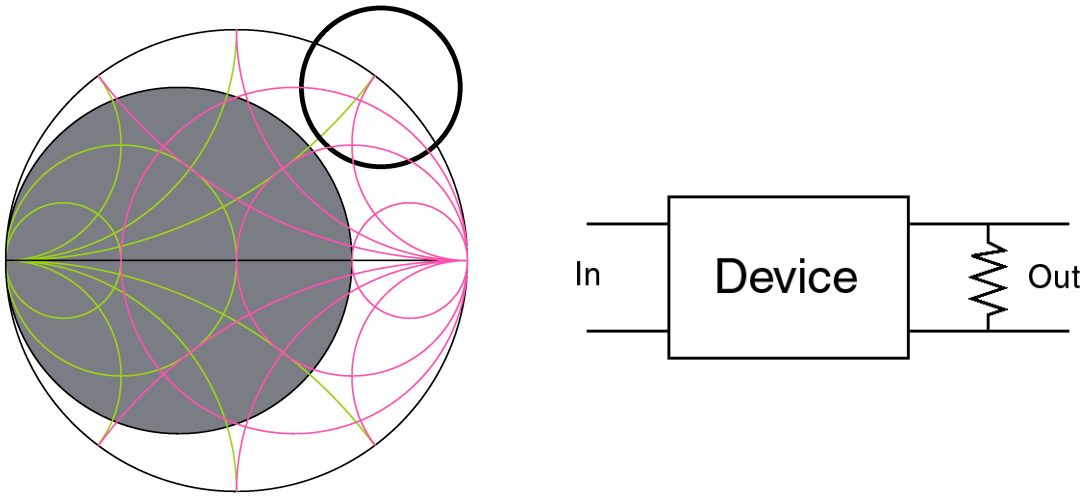


a) Resistive stabilisation principle. **b)** Resistive stabilisation circuit.

Figure 4.4 Resistive stabilisation.

If the stability is better at higher frequencies, which is usually the case, the effect of the resistor can be reduced at high frequencies, with a parallel capacitor. The parallel capacitor will then reduce the effective series resistance at higher frequencies.

4.2.3 Conductive Stabilisation



a) Conductive stabilisation principle **b)** Conductive stabilisation circuit.

Figure 4.5 Conductive Stabilisation

The conductive stabilisation is used at the output of the device to insure that the load impedance will never exceed a certain value. This is done by putting a resistor is parallel with the device. The shunt resistor restricts the achievable output impedance to the grey area in the Smith chart in Figure 4.5.

If the stability is better at high frequencies, the effect can be reduced as with the resistive stabilisation. For conductive stabilisation this is done by means of a series inductor. The series inductor will then increase the effective shunt resistance at the output node.

4.2.4 Feedback Stabilisation

The feedback stabilisation can be used as a supplementary to the other two methods. In

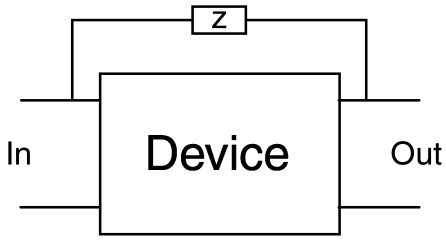


Figure 4.6 Feedback stabilisation.

addition to the stabilizing effect of feedback, the device will often be more linear than prior to the feedback.

4.3 Bias Circuit Instability

As mentioned above one cause of instability in a power amplifier is the matching of the device. Another cause is instability in the bias networks [3]. The instability in the bias networks is probably the most common source of oscillation in practical power amplifier designs.

To prevent instability caused by the bias circuit it is important to make sure the bias signal is filtered properly. An example of a bias circuit with low-pass filtering is shown in Figure 4.7.

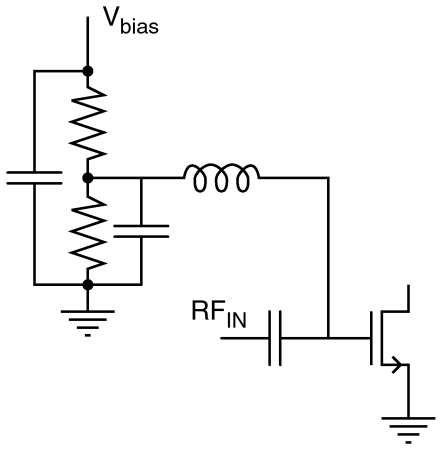


Figure 4.7 Example of stable bias circuit.

4.4 Verifying Stability through Simulations

It is very difficult if not impossible to prove during the design phase that a power amplifier is unconditionally stable in all operating conditions, but it is possible to give strong indications. In principle all of the following simulations must be performed at all operating conditions as well as all process corners. First of all the small-signal methods based on S-parameters described above will have to be applied to the power amplifier, but this will only reveal some of the potential problems and other methods will have to be introduced.

One of the ways to find instability is through transient simulations. Typically a node in the circuit is excited by a short pulse, this might start an oscillation in the circuit. If an oscillation is started it is observed whether the amplitude of the oscillation is rising or falling. If the amplitude rises a stability problems exists, if the amplitude is falling further investigation is needed. The energy in the pulse might then be changed or some of the operating conditions changed. If none of the modifications leads to an oscillation with rising amplitude the circuit is most probably stable. This procedure will have to be applied to all critical nodes in the circuits, especially the input port and the bias node.

Another method for revealing stability problems is focused on bias circuit stability. The method is the small-signal analysis described above, where the RF ports are analyzed based on the S-parameters. In addition to the RF ports the bias ports are

included in the S-parameter analysis. If not all ports are unconditionally stable over all frequencies from DC to well above the operating frequency a stability problem might exist.

4.5 Summary

Although it is possible to make a device unconditionally stable it is usually not desirable in a power amplifier, since it will have a rather large impact on the performance of the device. Instead the stability regions of the device is then compared with the expected input and output impedances of the device.

Unlike the single active device it is often impossible to prove a complete power amplifier to be unconditionally stable in the given operating conditions. It is however possible to get a reasonable reassurance through the simulation methods described above.

References

[1] L. Besser, "Avoiding RF oscillation," *Applied Microwave Wireless*, 1995.

[2] G. Gonzalez, *Microwave Transistor Amplifiers, Analysis and Design*. Prentice-Hall, 2 ed., 1997.

[3] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Artech House, 1999.

CHAPTER 5
CMOS TECHNOLOGY

The choice of technology is affected by a large number of parameters, such as maximum operating frequencies, substrate behavior, breakdown voltages, yield and cost. In the following the choice of CMOS for this project will be motivated. The modeling of CMOS transistors will be described along with some of the important features of the CMOS process such as the breakdown effects.

In the last part of this chapter the modeling of complete power amplifiers is discussed, this includes the passive components on-chip or off-chip as well as packages and PCBs.

5.1 Basic RF CMOS Behavior

The CMOS technologies are very cheap and are already used almost exclusively in the baseband part of a mobile phone. The most advanced CMOS technologies have gate lengths well into the deep submicron range. The maximum operating frequencies of these devices, are high enough for wireless RF applications. The main obstacles in CMOS are the low breakdown voltages and the large parasitics associated with the substrate. In the following section a simplified equation is given for the I-V characteristics of a MOS transistor including the knee voltage. The RF properties of a MOS transistor are rather complicated and will not be discussed here. The interested reader can find further information in [1].

5.1.1 I-V Characteristics

The I-V characteristics of a CMOS transistor is quite simple for long channels, but becomes complicated for short channels [1]. The strong inversion region is the most important operating region for transistors used in power amplifiers. The simple models divide the strong inversion into non-saturation and saturation. The boundary between non-saturation and saturation is given by:

$$V'_{DS} = \frac{V_{GS} - V_T}{\alpha} \qquad \textbf{(5.1)}$$

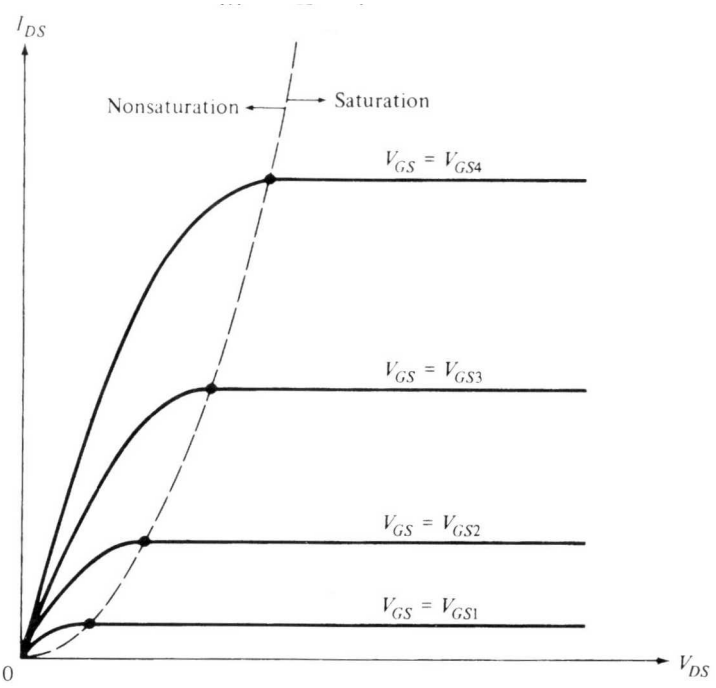


Figure 5.1 I-V characteristic of a typical submicron NMOS transistor [1].

where α is a process dependent parameter. This drain voltage is the same as the knee voltage discussed in Chapter 2. The drain current is given by:

$$I_{DS} = \begin{cases} \frac{W}{L}\mu C'_{ox}\left[(V_{GS}-V_T)V_{DS}-\frac{\alpha}{2}V_{DS}^2\right], V_{DS} \le V'_{DS} \\ \frac{W}{L}\mu C'_{ox}\frac{(V_{GS}-V_T)^2}{2\alpha}, V_{DS} > V'_{DS} \end{cases} \quad \textbf{(5.2)}$$

These equations are of course very crude, but gives an impression about the I-V characteristics of a MOS transistor used for power amplifiers. The I-V characteristics are illustrated in Figure 5.1.

5.1.2 Breakdown Phenomena

A number of breakdown mechanisms can occur in semiconductor devices, common to them all are that a large unwanted current starts flowing due to a high voltage applied to one of the terminals. With exception of the oxide breakdown the breakdown mechanisms are nondestructive, if the large currents are handled appropriately. The breakdown phenomena in question for power amplifiers are described below.

The PN junction breakdown effects are all initiated in the border region of the junction, when a sufficiently large reverse voltage is applied. If the circuit can handle the increased current, the breakdown is not destructive.

Avalanche Multiplication

The avalanche breakdown occurs in reverse biased PN junctions [2][3]. The avalanche breakdown causes the current to increase drastically. The voltage at which the avalanche breakdown occurs depend upon the doping profile of the junction, the breakdown voltage can be from a few volts to thousands of volts.

The avalanche breakdown is caused by some of the minority carriers gaining enough energy to break a covalent bond. This process known as impact ionization causes the creation of a new hole-electron pair. The creation of new hole-electron pairs increases the probability of impact ionization. This multiplication effect is why the phenomena is called avalanche breakdown.

Oxide Breakdown

The oxide breakdown is destructive in contradiction to the other forms of breakdown mentioned above [1]. The oxide breakdown occurs when a large voltage is applied over the gate oxide of a MOSFET. The effect on the transistor is a permanent short circuit through the insulator. The oxide breakdown can be caused by static charge, this means that ESD protective circuits must be used if an input is connected directly to the gate of a MOSFET.

Hot Carrier Effects

The hot carrier effects are not exactly a breakdown phenomena but rather a stress problem. The hot carriers are generated when carriers collide. The new carriers generated by the collisions are called hot carriers. If these carriers acquire enough energy they may cross the silicon-oxide barrier and cause damage in the gate-oxide. This causes aging of the CMOS devices, due to charges trapped in the gate-oxide [1].

5.2 Comparison to Other Technologies

Although the focus has been on CMOS till now a number of other technologies are available for the power amplifier designer. These technologies will be discussed briefly in the following sections.

5.2.1 SOI

The Silicon On Insulator (SOI) technologies are now almost mature, the properties are mostly the same as in CMOS, but the parasitics associated with the substrate are lower due to the insulator. This means the operating frequency is higher and the passive components will be better as well.

The breakdown voltage of an SOI transistor is dependent upon the type of the transistor. There are generally two types of transistors: thin-film and thick-film. In a thick-film transistor the region between the drain and the source is not fully depleted, and there will be a region controlled by the gate, one controlled by the substrate and a neutral

region in the middle. The neutral region forms an open-base parasitic bipolar transistor along with the drain and source.

In a thin-film transistor the region between the source and the drain are fully depleted and no neutral region exists. An open-base bipolar transistor has a rather low breakdown voltage, and this means that the breakdown voltage of a SOI transistor is even lower than that of a CMOS transistor. Besides the low breakdown voltages poor thermal conduction seems to be the largest problem.

5.2.2 LDMOS

The laterally diffused MOS (LDMOS) transistor is made of the same materials as the standard CMOS transistor, but with some important changes in the structure to allow for higher breakdown voltages. The main drawback of the LDMOS process is that the cost is higher than CMOS without gaining anything but higher breakdown voltages. The integration level is usually lower than in CMOS technologies.

5.2.3 GaAs MESFET

The GaAs MESFET transistors have previously been used extensively for power amplifiers, but now GaAs HBTs seems to be preferred. One of the main drawbacks of the GaAs MESFET processes is the relatively small wafers of typically four inches and the low yield which leads to a high cost. Furthermore the transistors are depletion mode devices, which implies the need of an additional negative supply voltages for biasing [4]. Due to the high resistivity substrate, the passive components are usually better than in CMOS technologies.

5.2.4 Silicon BJT

The silicon bipolar junction transistors (BJT) have a slightly higher cut-off frequency than an equivalent CMOS transistor. The cost of a pure bipolar process is a bit higher than CMOS. As is the case for all other technologies it is difficult to achieve the same level of integration as CMOS.

5.2.5 GaAs HBT

The Gallium Arsenide (GaAs) hetero-junction bipolar transistors (HBT) are widely used for RF power amplifiers. Compared to a normal bipolar transistor the transconductance and the cut-off frequency are higher. Typically no PNP devices are available in the process. The considerations about wafer size and yield are the same as for GaAs MESFET. As in GaAs MESFET technologies the passive components are decent [4].

5.2.6 SiGe HBT

The Silicon Germanium (SiGe) HBTs have been considered for power amplifiers, but problems arise with the relatively low breakdown voltages compared to GaAs HBT.

Otherwise the SiGe HBTs are placed between ordinary bipolar processes and GaAs HBTs with regard to performance as well as cost [5].

5.3 Simulation Models

There are a large number of simulation models available for MOS transistors, but only three of them are suitable for RF circuits. The three models are BSIM3, MOS9 and EKV, the foundations on which they are based are very different. Recently a fourth model has been introduced namely the BSIM4 model. The difference in foundations of the models gives rise to advantages and disadvantages when comparing the models. In the following sections the models will be described briefly.

5.3.1 BSIM3

The BSIM3 model started out as a physically based model, but over time it progressed into a more empirically based model with extra parameters for a lot of physical effects. The BSIM3 model is the most widely used model for analog circuits.

The BSIM3 model is backed up by the Compact Modeling Council (CMC) which is an industry association lead by the CAD vendors.

5.3.2 MOS9

MOS9 was from the beginning meant as an empirically based model, with the drawbacks and benefits of empirical models. The drawback is mainly that the model does not scale very well. The MOS9 model has earned a reputation as one of the best RF models, furthermore it is supposed to model noise more accurately than the other simulation models.

Although MOS9 is probably the best RF model now the future of the model seems short. The analytical models such as BSIM3, BSIM4 and EKV are preferred due to better ability to cover very different transistor geometries.

5.3.3 EKV

The EKV model was developed primarily by Enz, Krummebacher and Vittoz, hence the name. The EKV model can be considered a back to the basics model, compared to BSIM3 and MOS9.

The purpose of the EKV model is to provide a model which has a better transition from weak inversion to strong inversion. Furthermore the EKV model facilitate hand calculations on the same set of device parameters as for the precise CAD model.

Although very promising the EKV model has not yet reached a point at which the model can be considered mature enough for commercial applications.

5.3.4 BSIM4

BSIM4 is the latest model from UC Berkeley and is based on BSIM3, this means that the drawbacks and benefits of the BSIM3 is maintained. The most important improvement of the model is the inclusion of layout related information. This means that the BSIM4 model will be able to accurately predict the performance of e.g. a finger transistor. The layout information is layout type, number of fingers and related parameters.

As was the case for BSIM3 the BSIM4 model is supported by CMC, this means that BSIM4 will probably dominate the modeling scene in the years to come.

5.3.5 Layout Related Issues

In order to simulate the behavior of a MOSFET precisely it is necessary to add some information about the layout to the models. This is primarily done through the specification of the areas and perimeters of the drain and source regions of the transistor. In the simple case of a one finger transistor this is done easily, but the multifinger transistors are used the calculation gets more involved. The only model which handles these layout issues so far is the BSIM4 model.

Apart from the drain and source areas and perimeters the gate resistance is probably the most important parameter for RF designers. The gate resistance is usually not included in the transistor models from the vendor, it is therefore important to take into account. The gate resistance can be calculated by assuming that the effective resistance is equal to the resistance to the center of the gate [6].

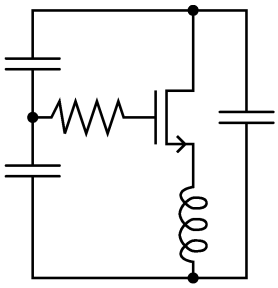


Figure 5.2 Enhanced RF MOS transistor model.

5.4 Modeling of Modules

The modeling of the RF transistors is not the only problem when modeling a power amplifier. A number of passive components will be placed on the chip as well as on the PCB. Furthermore modeling of the package is of importance to achieve good results.

5.4.1 Capacitors

The modeling of on-chip plate capacitors is relatively simple compared to the inductors, if care is taken during the layout phase. The capacitor can be modeled by the

intended capacitor, with an additional capacitor from the bottom plate to the substrate. A parasitic series resistance is associated with each of the two plates. Usually a careful design of the capacitor renders the used of a distributed model superfluous.

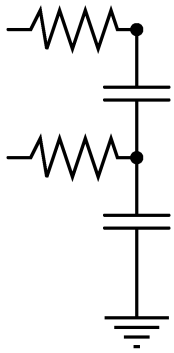


Figure 5.3 On-chip capacitor model.

Poly-poly capacitors are similar to metal-metal capacitors, but since the plates are made of polysilicon instead of metal the series resistance associated with the capacitors are typically 10-50 times larger than for metal-metal capacitors. This can to some extent be reduced by designing the capacitor very carefully, but the performance will never be as good as metal-metal capacitors.

Apart from the plate capacitors a number of other capacitors are available in a CMOS process. Most commonly used is the MOS capacitor made up by the gate-oxide. Due to the very thin gate-oxide the density of MOS capacitors is very high, but one of the terminals have to be grounded. Since the density is high and one of the terminals is grounded the MOS capacitors are used primarily for decoupling. The modeling of the MOS capacitors is simply an ordinary MOS transistor with drain, source and bulk connected as on of the terminals and the gate as the other terminal.

5.4.2 Spiral Inductor

Over the last couple of years a lot of research effort has been put into the characterization and modeling of the on-chip inductors. Although no satisfactory solution is yet available it is now possible get good models of the inductors during the design phase.

Almost all of the models are based on a Π network as shown in Figure 5.4. One of the more complete inductor models is shown in Figure 5.5 [7].

Some foundries have included scalable inductor generators and models in their design kits. For instance STMicroelectronics has a scalable model based on Figure 5.5. Using this approach the use of on-chip inductors is greatly simplified for the designer.

5.4.3 Interconnects

One of the important things when trying to simulate a complete chip is to maintain the overview. If all interconnects were modeled regardless of their impact on the performance, the simulation speed would increase drastically and hence prevent

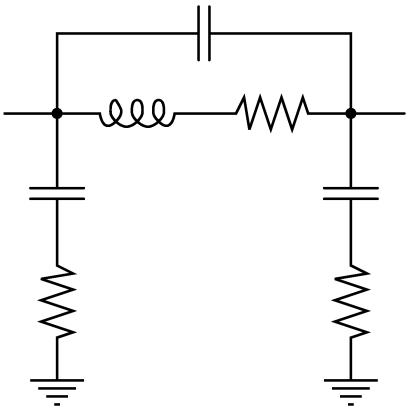


Figure 5.4 Simple Π network inductor model.

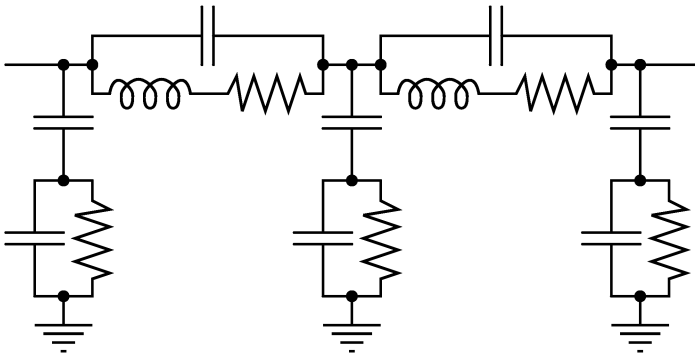


Figure 5.5 On-chip inductor model.

simulation of the complete chip. It is therefore important to carefully select which interconnects should be modeled. In most cases it is sufficient to model the interconnects with RLC networks. A simple model of a metal wire is shown in Figure 5.6.

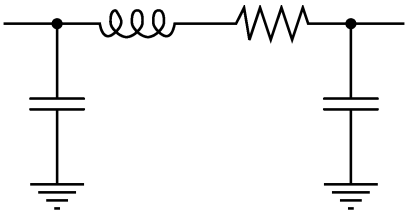


Figure 5.6 Simple RLC network metal wire model.

5.4.4 Packaging

There are generally two different packaging topologies, the ordinary chip package usually in plastic and the chip-on-board approach (COB). The package contains the leadframe of the package as well as the bondwires, while the COB approach only contains bondwires.

The bondwires are an important part of the entire RF design. The bondwires have inductance, capacitance and resistance associated with them. The self-inductance of a bondwire is [8]:

$$L = 0.2 \cdot 10^{-6} \cdot l\left[\ln\left(\frac{2l}{r}\right) - \frac{3}{4} + \frac{r}{l}\right]H \qquad \textbf{(5.3)}$$

where l is the length of the wire and r is the radius of the wire. The mutual inductance between the two parallel bondwires of equal length is:

$$M = \frac{l}{5}\left[\ln\left(\frac{l}{d} + \sqrt{1 + \left(\frac{l}{d}\right)^2}\right) - \left(\sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l}\right)\right]H \qquad \textbf{(5.4)}$$

where d is the distance between the wires.

Using these two and related formulas it is possible to calculate the complete inductance of the wires used for a single signal as well as the coupling to other signals. More complicated equations exists for the mutual inductance of bondwires not parallel and of different length [8]. Using these equations it is also possible to model the bondwires in the package.

The leadframe is usually characterized using a electro-magnetic finite-element simulator, a lumped model is then extracted from the simulator. In Figure 5.7 an example of the package model is shown for a single pin. Between the different pins capacitive as well as inductive couplings exist as sketched in the figure.

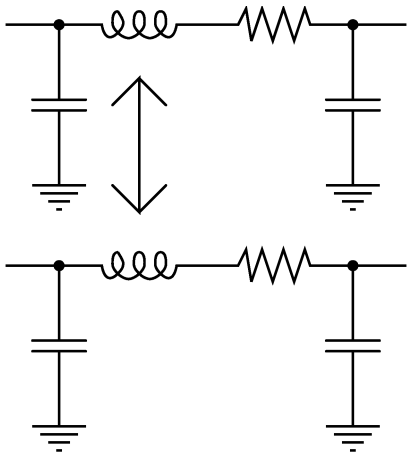


Figure 5.7 Leadframe model for two adjacent pins.

5.4.5 PCB

The PCB is modeled using microstrips. In some simulators e.g. APLAC, a number of microstrip components are implemented. If the microstrips elements, e.g. Tees and Stubs, are not implemented is possible to make macromodels for them, as long as the basic microstrip is implemented in the simulator.

Another part of the PCB modeling is the passive components used in e.g. the output matching network. Usually the vendors of the SMD components deliver frequency dependent models of their components. These models are usually sufficient to get accurate simulations.

5.4.6 Thermal Modeling

In power amplifier modeling it is important to include the thermal effects of the power dissipation in the transistors. The thermal network is modeled with equivalent current sources, capacitors and resistors modeling the heat generation, thermal capacity and thermal resistance respectively [9][10][11]. A very simplified thermal model of the power amplifier is shown in Figure 5.8.

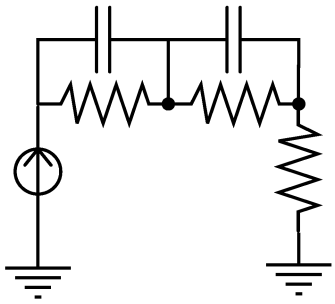


Figure 5.8 Simplified thermal model of a power amplifier.

5.5 Summary

A number of technologies with very different properties are available for power amplifier designers. The CMOS technology is very attractive in low-cost designs as well as highly integrated transceivers.

The cost of a CMOS power amplifier is probably always going to be the lowest possible, since the production cost and yield is better than any other technology, furthermore the integration level is also very high.

The low breakdown voltages of CMOS is a problem compared to some of the other technologies in question, but the low voltage performance of the transistor is better than most other technologies. This means that a CMOS power amplifier can be operated on the same supply voltages as the digital logic in the baseband part of the transceiver.

The modeling of RF power amplifiers is very troublesome, if accurate results are expected. It is however possible to accurately model the power amplifiers by using the models described in this chapter.

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CHAPTER 6

DESIGN METHOD FOR INTEGRATED POWER AMPLIFIERS

The design of power amplifiers has so far involved some amount of black magic performed by experienced RF designers. A large part of this work has focused on removing at least some of the black magic in power amplifier design. During the design process a lot of choices will have to be made, if just one of the choices are wrong the whole project is in jeopardy. The following design method will try to formalize the decision process. A number of design methods have previously been published but have all focused on single stage power amplifiers [1][2][3][4][5][6].

The design process starts at the output stage of the power amplifier, since this stage will influence the rest of the power amplifier. The design will therefore start at the output load and work backwards through the power amplifier.

The overall design flow is illustrated in Figure 6.1. As can be seen from the figure the design flow is divided into three major parts. In *Initial Design Decisions* decisions about differential or single-ended operation and the number of amplifying stages are made. In *Stage Design* the individual stages of the power amplifier are designed. In *Combination of Stages* the designed stages are combined. After the combination of the individual stages the complete power amplifier is evaluated. If the result is not satisfactory the individual stages are redesigned.

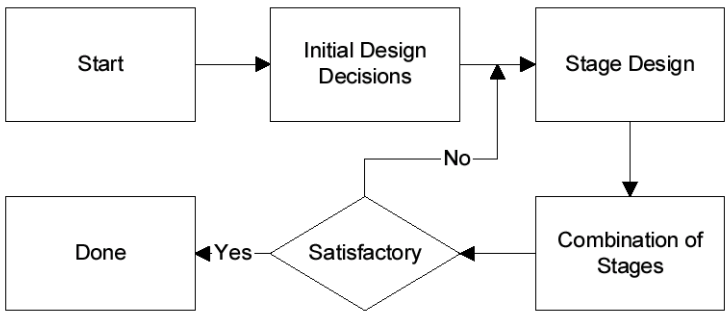

Figure 6.1 Overall design flow.

6.1 Initial Design Decisions

Before the actual design of the power amplifier starts a number of initial decisions will have to be made. This includes the choice of the single-ended or differential operation, the number of stages and a budget for gain and efficiency. The design flow for the initial design decisions is shown in Figure 6.2.

Figure 6.2 Design flow for initial design decisions.

6.1.1 Differential or Single-ended Operation

As discussed in Chapter 2 there are a number of benefits and drawbacks of differential operation of the power amplifier. The choice between single-ended and differential operation will always be a trade-off between a number of different factors. It is also possible to switch between differential and single-ended operation somewhere in the power amplifier chain.

6.1.2 Number of Stages

The next decision to make is to decide on the number of stages in the power amplifier. The number of stages is restricted by a number of requirements. The total gain necessary along with the maximum gain of a single stage sets the absolute minimum number of stages. The isolation obtainable in each stage and the total isolation needed also sets a lower limit. Power control is another example that may increase the minimum number of stages, but additional stages increase the cost and complexity of the power amplifier and it is therefore desirable to keep the number of stages low. Another upper limit is set by the total efficiency of the power amplifiers, since each extra stage will lower the total efficiency of the power amplifier.

6.1.3 Gain & Efficiency Budget

To be able to design the individual stages in the following steps, it is necessary to have information about the behavior of the individual stages. A budget is therefore made for key parameters like gain and efficiency of the stages.

6.2 Design of Individual Stages

After the initial design decisions have been made, the actual design of each stages in the power amplifier starts. The first stage to be designed is the output stage, since most of the characteristics of the power amplifier will be derived from this stage. The necessary output power from the preceding stage is also determined by the output stages. This

means that it is most rational to work backwards through the chain and start with the output stage and stop with the input stage. In some applications however it will be more convenient to start with the output stage then design the input stage and at last design the remaining stages.

The design flow for the design of the individual power amplifier stages is shown in Figure 6.3. First of all the class of operation is selected, then the transistor is designed and at last the load and source impedance matching network are designed.

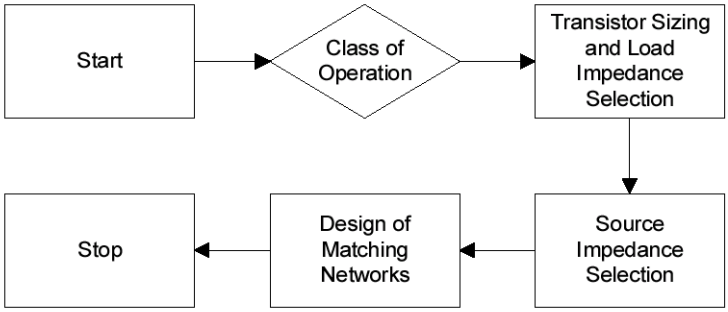

Figure 6.3 Design flow for individual stage design.

6.2.1 Class of operation

The choice of class of operation is the first decision to make in the design of the stage. As described in Chapter 2 the mode of operation influences almost all parameters of the power amplifier including linearity, gain and efficiency.

The class of operation of each stage is a trade-off between a number of factors. The factors include linearity, power gain, efficiency, breakdown voltage and load impedance. The individual stages of the power amplifier do not necessarily all operate in the same class.

First of all the linearity requirements must be fulfilled for very high linearity requirements such as that for base station power amplifiers class A will be a natural choice. On the other hand constant envelope standards like GSM have very low linearity requirements and most modes can be used. The newer standards such as EDGE and WB-CDMA is placed somewhere in between and class AB could be a reasonable choice.

The efficiency and gain is the next thing to take into account. Although the drain efficiency is in theory higher for reduced and switching mode amplifiers, the power added efficiency may not differ that much due to the relatively low power gain of these classes, this is especially true for low gain devices with 9-12 dB gain.

Another thing to take into account is the breakdown voltage of the output transistor, this is especially true for CMOS, where the destructive breakdown of the gate-oxide occurs at a relatively low voltage. Class C and E will results in voltage swings of 3-5 times the supply voltage. While class A, AB and B only have double voltage swing.

6.2.2 Transistor Sizing and Load Impedance Selection

An initial guess of the transistor size originates from the I-V characteristic of the transistor. After an initial value is selected the more accurate RF behavior is found using load-pull simulations. The design flow for transistor sizing and load impedance selection is illustrated in Figure 6.4.

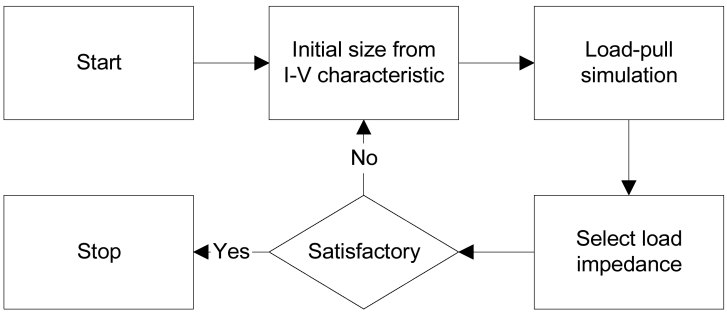

Figure 6.4 Design flow for transistor sizing and load impedance selection.

The load-pull simulations are the simulation equivalent of the load-pull measurements [7]. The load-pull simulation determines not only the transistor size but also the load impedance. In practice the load-pull simulation sweeps a range of impedance points and draws e.g. power, efficiency and linearity contours. This is done with either an ideal load impedance or a matching network with the desired topology. If the matching network is chosen it will have to be synthesized at each impedance point, but the results resembles the actual performance more closely. The load impedance is then chosen as a trade-off between e.g. output power, efficiency and linearity. The load-pull simulations are described in more detail in Chapter 3. The impedances at harmonic frequencies are part of the definition of the mode of operation and is therefore defined by the selection of the class of operation.

6.2.3 Source Impedance Selection

The source impedance can be found using the small-signal impedance matching methods described in Chapter 3 [8]. Using one of the small-signal method with the load impedance found in the previous step, a single source impedance will be given. It is also possible to use a source-pull simulation in the same way as the load-pull simulation.

6.2.4 Design of Matching Networks

If the matching network topology was already chosen for the load-pull simulation it will only have to be synthesized. In the synthesis it is necessary to take all the important parasitics into account, this can be omitted in the initial load-pull simulations.

Based on the choice of impedance at fundamental and harmonic frequencies the output matching network is designed. An important part of the output matching network is the biasing, e.g. supply voltage. The topologies of the matching networks and the synthesis of them have been described in Chapter 3.

When selecting the matching network topology the biasing of the stages is often an important part. Selecting the right topology will give DC blocking and biasing at the same time as the impedance matching.

Depending on the mode of operation the optimal drive conditions for the output stage may differ. In the design of the input matching network biasing will also have to be incorporated, either as an integrated part of the matching network or explicitly, the latter will then have to be considered as a parasitic in the input matching network.

6.3 Combination of Stages

The final part of the power amplifier design is to combine the individual stages and the input matching networks will have to be merged with the output matching networks of the preceding stage. Then the stability of the complete power amplifier will have to be examined. This is done using transient simulations and small-signal stability analysis. The small-signal analysis uses all ports, DC or RF, as RF ports and the stability is then analyzed [7].

The design flow for the combination of the individual power amplifier stages is shown in Figure 6.5.

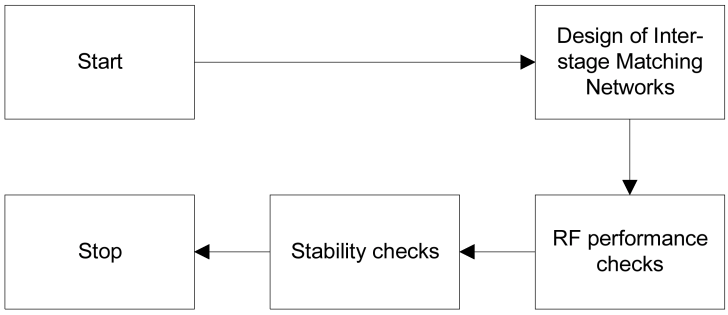

Figure 6.5 Design flow for combination of individual stages.

6.3.1 Design of Interstage Matching Networks

The design of the interstage matching networks will be based on the output matching network of the preceding stage and the input matching network of the following stage. It is often possible to reduce the number of passive components compared to the total number of components used in the two initial networks. In integrated power amplifiers the passive components often dominate the die size as well as the losses in the power amplifier. It is therefore often desirable to minimize the number of passive components.

The design of the interstage matching networks is an iterative process where the performance is verified continuously by a large-signal simulator. Based on the simulated results the interstage matching network will be optimized.

6.3.2 Check RF Performance of Power Amplifier

After the interstage matching networks have been designed it is necessary to simulate the complete power amplifier to verify the output power and efficiency. Usually it will then be advantageous to fine tune the matching networks in an iterative process to optimize the key parameters.

The RF performance is verified by steady-state and transient simulations. These simulations will have to cover the different process corners, the discrete component tolerances as well as the complete operating temperature.

6.3.3 Check Stability

When the RF performance is verified the stability of the complete power amplifier is checked. The first check is the in-band stability, these checks have been described in Section 4.2. Then the bias stability is verified as described in Section 4.3.

The stability is checked by small-signal and transient simulations. The input, output and bias ports are all treated as RF ports in the small-signal simulations. The transient simulations use pulses to excite the circuit to provoke oscillations. As was the case for the RF performance verification all simulations will cover process corners, component tolerances and the entire temperature range.

6.4 Summary

In this chapter a design method for integrated power amplifiers was presented. This design method was developed and used through the design of the power amplifiers in Chapter 8.

The design method describes the design of an RF power amplifier from specification to the finalized design. Although the design has been formalized the designer still has to make the decisions, but the formalized decision process ensures that the choices are made in the right order.

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CHAPTER 7
DIGITAL PREDISTORTION

As mentioned in Chapter 1 some of wireless communication standards require linear power amplifiers. The IS-95 standard which is used primarily in North America is one of those standards and sets limitations on the ACPR allowed. These requirements can be met by using either a linear power amplifier with relatively low efficiency or by introducing linearization. One of the linearization methods is digital predistortion which can be implemented without decreasing the efficiency of the usually effective nonlinear power amplifiers.

To demonstrate the feasibility of digital predistortion a solution has been implemented for an already existing power amplifier. The power amplifier used was designed by Gary Hannington at University of California, San Diego for the IS-95 system.

In the IS-95 system the output power of the handset is usually substantially lower than the maximum output power. The probability of each power level has been plotted along with the efficiency of an ordinary class A power amplifier in Figure 7.1. As can be seen from the figure the power amplifier hardly ever operates at maximum output power and thereby maximum efficiency.

The power amplifier was implemented using GaAs MESFET transistors and operates at a carrier frequency of 950MHz. The output power of the power amplifier is controlled by supply voltage modulation. In the dynamic supply voltage (DSV) power amplifier, a DC-DC converter is used to adjust the power supply voltage provided to the output stage in accordance with the output signal level. This architecture can provide a significant increase in overall efficiency, particularly if the amplifier is operated at relatively low output power during a substantial fraction of the time [1]. The schematic of the (DSV) power amplifier is shown in Figure 7.2.

The total efficiency of the power amplifier increases substantially at output powers below the maximum output power compared to a conventional power amplifier. The total efficiency including the DC-DC converter has been plotted as a function of output power in Figure 7.3.

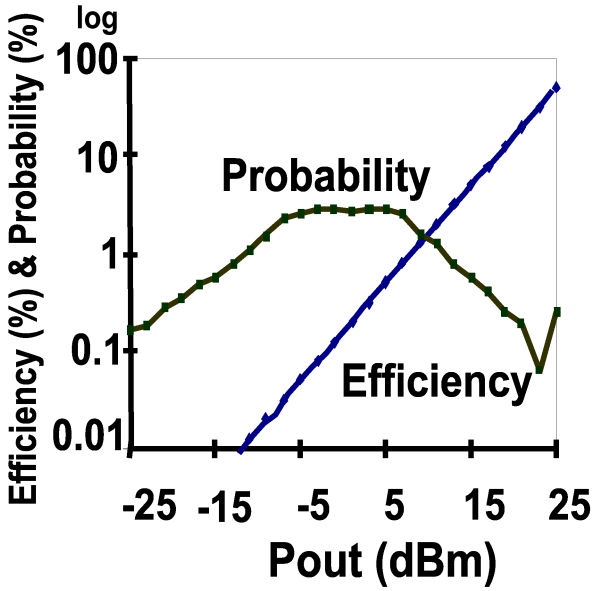

Figure 7.1 Probability and class A efficiency vs. power levels.

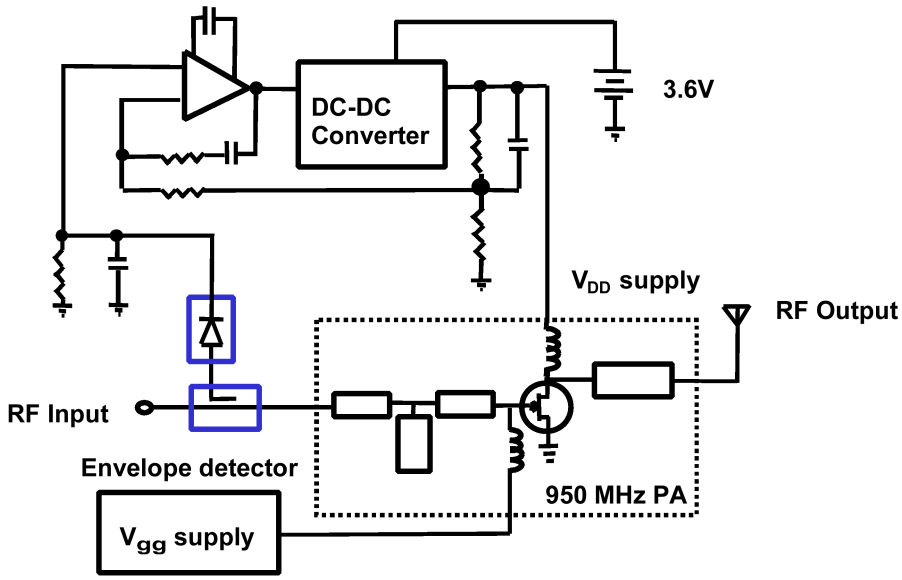

Figure 7.2 Schematic of dynamic supply voltage power amplifier.

The probability from Figure 7.1 can be combined with the efficiencies from Figure 7.3 as illustrated in Figure 7.4. If the effective efficiency based on the probabilities is calculated it can be seen that the same power amplifiers total efficiency increases by a factor of 1.4 when the dynamic supply voltage is used.

It has been found, however, that the output linearity can be degraded in the DSV system. The reduced linearity results from a variation in amplifier gain as the supply voltage is varied. In previous work, it has been shown that by dynamically varying the gate bias in a MESFET-based DSV amplifier along with the power supply voltage (drain bias, V_{DD}), the linearity of the amplifier can be restored [1]. In this work the linearization of the DSV amplifier is done by predistorting the signal fed to the amplifier, in a manner that can be accomplished with digital signal processing. Using a MESFET-

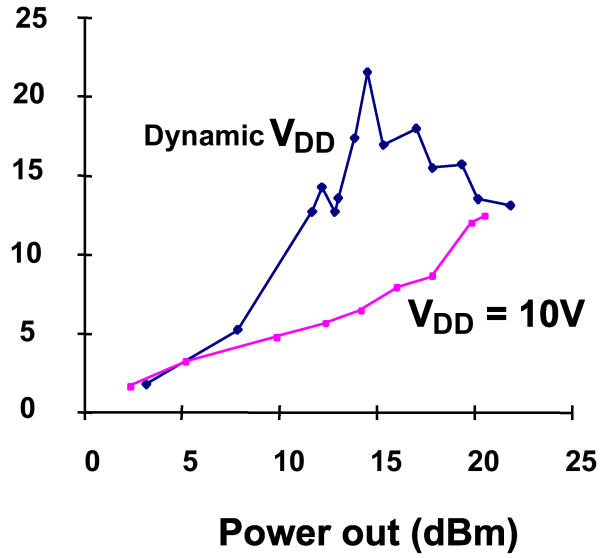

Figure 7.3 Total efficiency as a function of the output power.

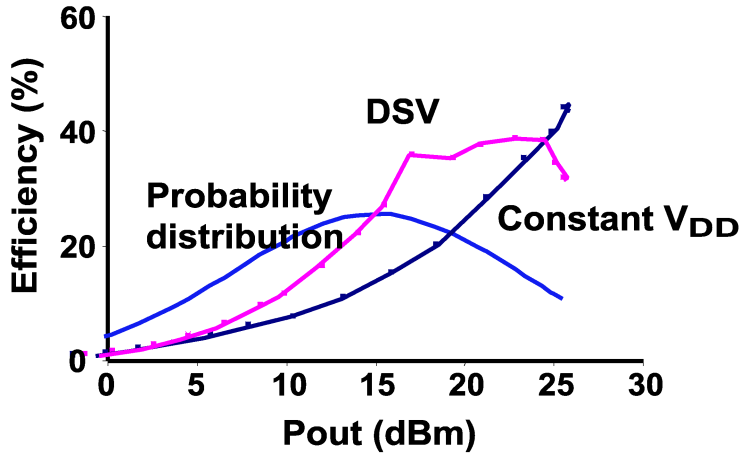

Figure 7.4 Probability and efficiency combined.

based DSV amplifier with DSP-based linearization the ACPR requirements of IS-95 is met.

7.1 Theory of Digital Predistortion

The theory behind digital predistortion is based on memory-less bandpass nonlinearities. To be able to implement the predistortion system it will also be necessary to have basic information about the modulation format of the communication standard. In the following section the modulation and the modeling and predistortion of the nonlinearities will be described.

7.1.1 Digital Modulation of IS-95 Signal

The digital modulation used in IS-95 is based on offset quadrature phase shift keying (OQPSK). OQPSK is one of the quadrature modulation formats, which are based on sin

$\omega_c t$ and cos $\omega_c t$ being orthogonal functions. Compared to conventional QPSK there are no 180º phase transitions in OQPSK this means that there are no crossings through zero. The zero crossings are usually difficult to handle in high efficiency power amplifiers due to the amplitude going through zero. Since the requirements for the power amplifier are lower than for QPSK, OQPSK are often favored in handsets. The phase transitions of QPSK and OQPSK modulation formats can be represented in a constellation diagram as shown in Figure 7.5 [2][3].

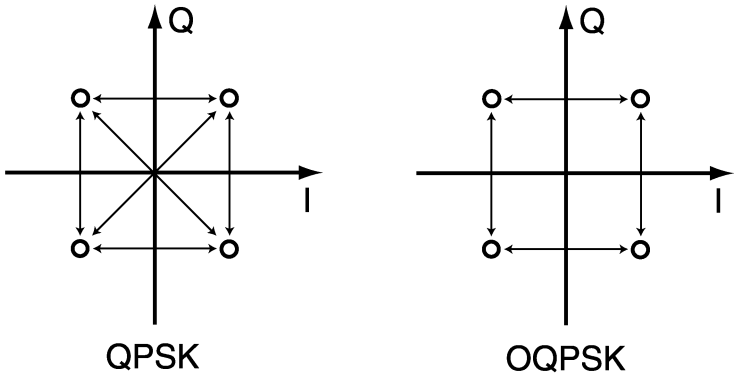

Figure 7.5 Constellation diagram showing phase transitions in QPSK and OQPSK.

A simple digital OQPSK modulator is shown in Figure 7.6. First the serial bit-stream is parallelized. Then the two bits are passed through the two separate branches I and Q. The Q signal will be delayed by half the symbol period. The two signals are low-pass filtered to limit the output spectrum before they are upconverted with mixers to the carrier frequency. The LO input of the I branch is a sine waveform while the Q branch uses a cosine waveform. Finally the two separate branches are combined using an adder.

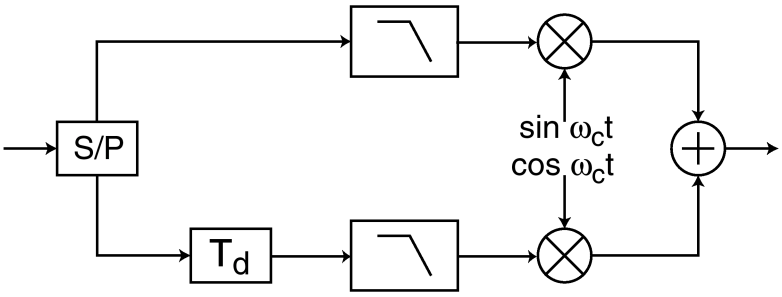

Figure 7.6 Block diagram of digital OQPSK modulation.

All of these blocks are easily implemented using a DSP. The low-pass filters are usually constructed as FIR filters while the rest of the components are basic arithmetic functions.

7.1.2 Modeling of Nonlinearities

The nonlinearity of a narrowband power amplifier can be modelled quite accurately using memory-less bandpass nonlinearity theory [4]. This may seem like a limitation, but in practice all wireless modulation standards, can be regarded as narrowband, compared to the carrier frequency. To model the behavior of a power amplifier the CW AM-AM and AM-PM characteristics are measured. These data can then be used in a

baseband model of the power amplifier. A narrowband modulated signal can be represented by:

$$x(t) = A(t) \cdot e^{j[2\pi f_0 t + \phi(t)]} \quad \textbf{(7.1)}$$

where A(t) is the amplitude of the signal as a function of time while $\phi(t)$ is the phase of the signal.

$$x_{dist}(t) = A_{dist}[A(t)] \cdot A(t) \cdot e^{j[2\pi f_0 t + \phi(t) + \phi_{dist}[A(t)]]} \quad \textbf{(7.2)}$$

where $A_{dist}(x)$ is the amplitude distortion, i.e. the difference between wanted and actual amplitude, as a function of input power and $\phi_{dist}(x)$ is the phase distortion as a function of amplitude. This can be rewritten as:

$$x_{dist}(t) = A_{dist}[A(t)] \cdot e^{j\phi_{dist}[A(t)]} \cdot x(t) \quad \textbf{(7.3)}$$

7.1.3 Predistorting a Nonlinear Signal

To predistort the signal is the distortion has to be inverted:

$$x_{pre}(t) = \frac{1}{A_{dist}(t)} \cdot e^{-j\phi_{dist}(t)} \cdot x(t) \quad \textbf{(7.4)}$$

For an efficient DSP implementation, it is necessary to do the predistortion at baseband, and operate separately on the I and Q signals. The equations for the predistorted I and Q signals are:

$$I_p = \frac{I \cdot \cos\Phi_{dist} + Q \cdot \sin\Phi_{dist}}{A_{dist}(A)} \quad \textbf{(7.5)}$$

$$Q_p = \frac{Q \cdot \cos\Phi_{dist} + I \cdot \sin\Phi_{dist}}{A_{dist}(A)} \quad \textbf{(7.6)}$$

7.2 Implementation

The implementation consists of a signal generator and a piece of software for data generation. In this implementation, the I and Q channels outputs were precomputed in software for a specific pseudorandom output data pattern, and fed to the system with a signal generator which allows arbitrary I and Q waveforms to be specified.

The generation of the data is done using a C++ program. The digital predistortion method presented here can be implemented effectively in a DSP.

7.2.1 Equipment

The equipment used for the project is a HP ESG-D signal generator. The signal generator generates I and Q signals, which are then IQ upconverted to a RF frequency between 250 kHz and 4 GHz.

This signal generator is equipped with an option, which will allow an arbitrary I and Q waveforms to be specified. The arbitrary waveforms can contain 1 Msample per channel and the sampling frequency is between 1 sample/s and 40 Msamples/s. The waveform data consists of 14 bits per sample per channel.

The arbitrary waveforms are generated on a computer and then transferred to the signal generator through a GP-IB bus.

7.2.2 Data Generation Software

The generation of the data is done, using a C++ program. The C++ program will also simulate the behavior of the amplifier with or without the predistortion. The simulation is done with measured AM-AM and AM-PM distortion data. The predistorted I and Q waveform are quantized to 14 bits as required by the signal generator.

The digital predistortion presented here can be implemented very effectively in an already existing DSP. The overhead for implementing the predistortion is six multiplications and two additions as well as 40-100 data entries in a table, all of the above could be implemented as integer operations. In an IS-95 implementation with four times oversampling this equals approximately 30 MIPS, compared to the several hundred MIPS available in modern DSPs. The memory required would be 80-200 bytes.

7.3 Measurements

First of all the AM-AM and AM-PM characteristics have to be measured, this can be done in several ways, but the easiest solution is to use a vector network analyzer. The network analyzer is setup for a power sweep, and the gain and phase is retrieved from the S_{21} data. The measurement setup for getting the AM-AM and AM-PM data is shown in Figure 7.7.

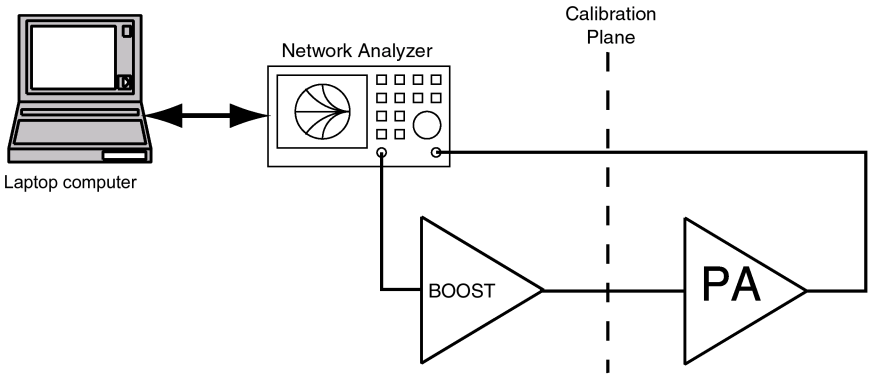

Figure 7.7 Measurement setup for retrieving AM-AM and AM-PM data.

These tables are put into the data generation program. An OQPSK signal is generated and filtered according to the IS-95 standard. At this point the predistortion is applied and the I and Q signals are then transferred to the signal generator. The signal generated by the signal generator is passed through a pre-amplifier, to generate high enough input power.

The measurements of the ACPR is done using a spectrum analyzer, this can be done using either a built-in function for the ACP calculation, or by transferring the spectrum to a computer and do the calculations there. It is however necessary to do some averaging of the results, regardless of how they are acquired. The setup for measuring the ACPR of the digital predistortion system is shown in Figure 7.8.

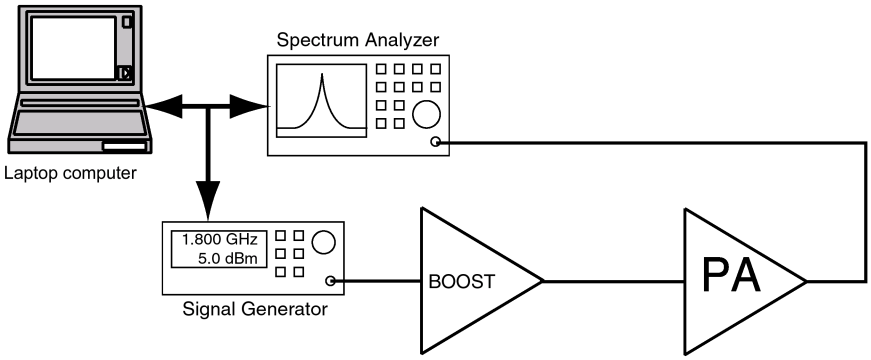

Figure 7.8 Measuring ACPR for digital predistortion system.

Measurements of the ACPR were done using a spectrum analyzer. A built-in function for the channel power calculation was used and the result was transferred to a computer and used for ACPR calculations. Averaging of results over many runs was done to obtain accurate values. Measurements have shown an improvement of the ACPR of the power amplifier described above on the order of 4-6 dB, as shown in Figure 7.9.

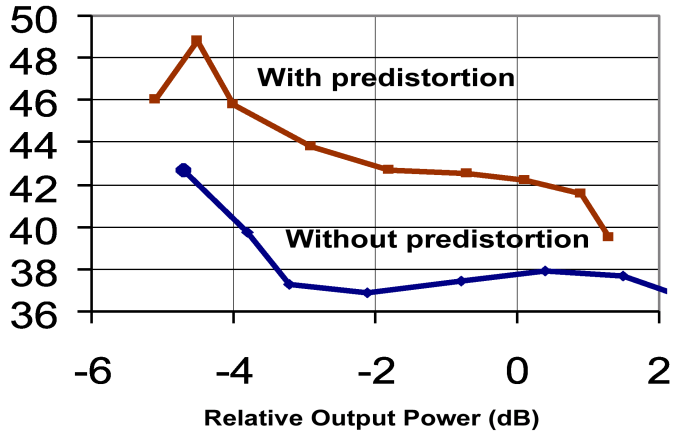

Figure 7.9 ACPR measurements with and without digital predistortion.

The output spectrum with and without predistortion is shown in Figure 7.10. The resulting output spectrum is capable of meeting IS-95 requirements. As a result of the improved linearity of the power amplifier system, it was possible to increase the output power by 4dB. The predistortion also means that the amplifier can be driven further into compression, thereby achieving a higher efficiency.

7.4 Continued Work

After the initial digital predistortion system was completed the work continued in directions suggested by the author. The author has been in continuos contact with UCSD

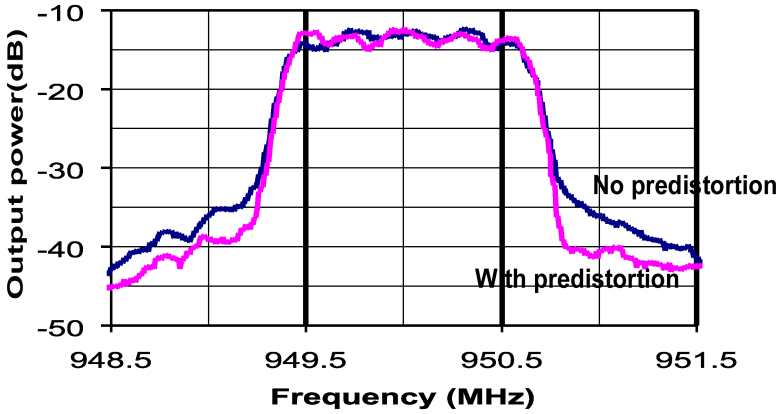

Figure 7.10 The output spectrum of the DSV power amplifier with and without digital predistortion.

and discussed implementation details. The improvements of the digital predistortion system were mainly targeted at the dynamic supply voltage power amplifier used at UCSD. Along with the digital predistortion described here the control of the DC-DC converter was handed over to the DSP.

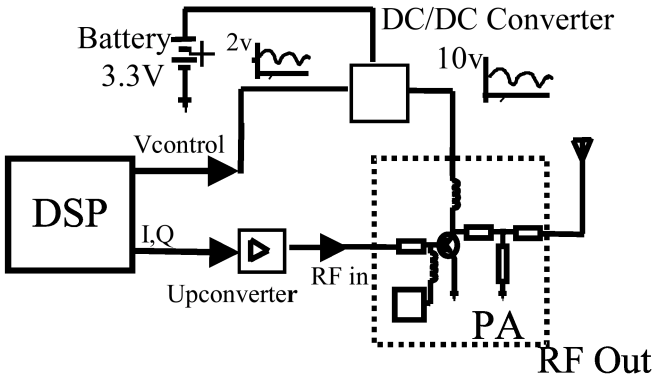

Figure 7.11 Schematic of improved digital predistortion system.

By removing the envelope detector and controlling the DC-DC converter directly from the DSP it was possible to eliminate the delays in the control loop. The effect of adding a delay in the DC-DC converter control loop has been simulated and the results of different delays are shown in Figure 7.12. When controlling the DC-DC converter directly no memory effects remain in the system.

The ACPR was improved by 8dB compared to a system without predistortion. The results of this improved digital predistortion system are shown in Figure 7.13 [5].

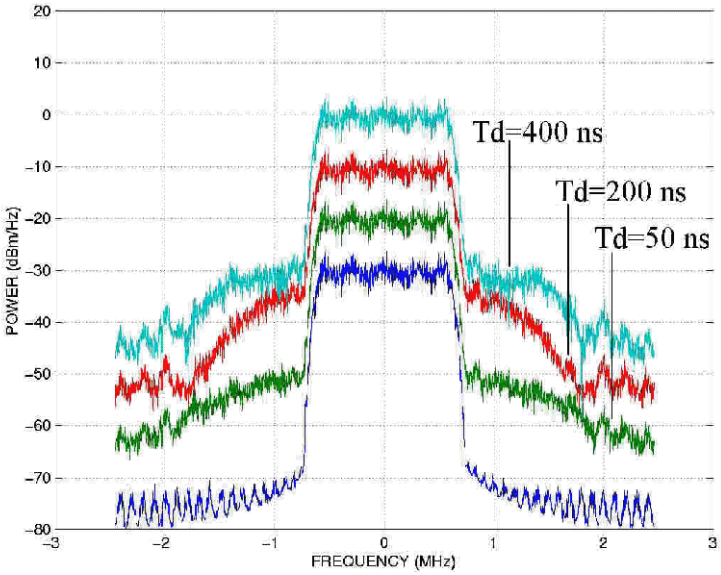

Figure 7.12 Effect of delay in DC-DC converter control loop.

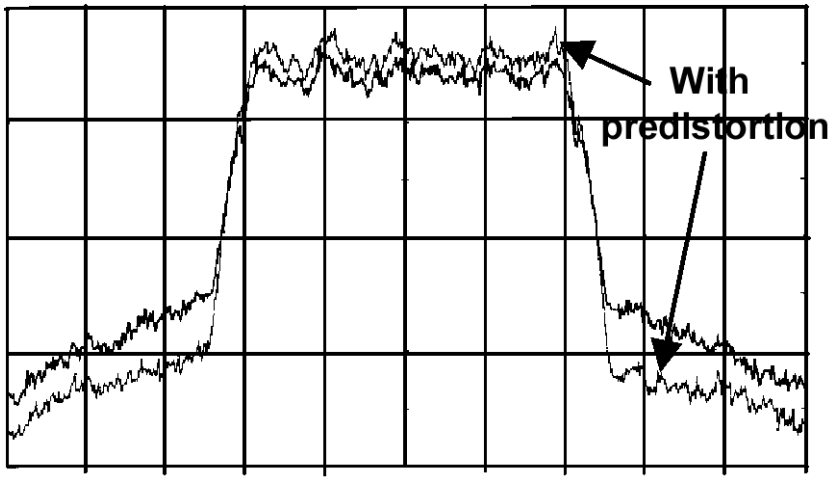

Figure 7.13 Spectrum of improved digital predistortion system.

7.5 Summary

In simulations it is possible to obtain full linearization up to a certain output power level. In practice this will not be the case. It has however been proven that the predistortion will improve the linearity of the power amplifier.

Measurements have shown an improvement of the ACPR of the power amplifier described above of 6-8dB depending on the implementation. These improvements may be the difference between passing the ACPR tests or not. It also means that the amplifier can be driven further into compression, thereby achieving a higher efficiency. The results have been presented in [6][7] while the continued work has been presented in [5].

References

[1] G. Hanington, P. F. Chen, V. Radisic, T. Itoh, and P. M. Asbeck, "Microwave power amplifier efficiency improvement with a 10 MHz HBT DC-DC converter," in *1998 IEEE MTT-S Intl. Microwave Symposium Digest*, vol. 2, pp. 589--592, 1998.

[2] B. Razavi, *RF Microelectronics*. Prentice Hall, 1998.

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[4] M. C. Jeruchim, P. Balaban, and K. S. Shanmugan, *Simulation of Communication Systems*. Plenum, 1992.

[5] M. Ranjan, K. H. Koo, G. Hanington, C. Fallesen, and P. Asbeck, "Microwave power amplifiers with digitally-controlled power supply voltage for high efficiency and high linearity," in *2000 IEEE MTT-S International Microwave Symposium*, (Boston, USA), June 2000.

[6] C. Fallesen, G. Hanington, and P. M. Asbeck, "Improved linearity of a dynamic supply voltage power amplifier using digital predistortion," in *1999 IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, (San Diego, USA), September 1999.

[7] P. M. Asbeck, G. Hanington, M. Ranjan, L. Larson, C. Fallesen, and H. Finlay, "Envelope tracking or dynamic supply voltage power amplifiers for wireless communications," in *Efficiency and Linearity Enhancement Methods for Portable RF/MW Power Amplifiers Workshop*, (Boston, USA), June 2000.

CHAPTER 8

DESIGN OF CMOS POWER AMPLIFIERS

Three CMOS power amplifiers have been designed to demonstrate the feasibility of CMOS power amplifiers for wireless communication. To lower the risk of the designs a gradual approach was chosen where the first power amplifier was a rather simple two stage amplifier with external bias circuit. The third power amplifier was highly integrated compared to other solutions published so far.

The power amplifiers were all designed for the STMicroelectronics BiCMOS6G process which is a 0.35 μm bulk BiCMOS process with a substrate resistivity of 10-20 Ω-cm. Although most digital CMOS processes uses low resistivity epitaxial substrate to prevent latch-up, it is possible to get medium resistivity bulk CMOS processes from a number of foundries including STMicroelectronics, AMS, TSMC and UMC. The main contribution of the bulk substrate is reduced losses in the on-chip inductors compared to the standard epi-substrates.

The process has 5 metal layers although the first design was carried out in a version with only four layers. The top metal layer is 2.5 μm thick, which is four times the thickness of the remaining layers. This is consistent with the thick power supply rails in modern digital CMOS processes.

The process has thin-oxide metal-metal capacitors involving one extra processing step. The thin-oxide metal-metal capacitors have a high density and therefore the die size (cost) of the complete power amplifier can be reduced. Apart from the thin-oxide metal-metal capacitors a scalable inductor device generator and corresponding model is available directly from the foundry.

The CMOS process used for the prototypes is actually a BiCMOS process. The bipolar parts of the process is, however, not used. The reason for choosing the BiCMOS process was mainly the availability of design-kit and transistor models which were mature for RF design. A number of foundries now offers pure CMOS processes on bulk substrate with metal-metal capacitors and a thick metal layer. ´

The two first prototypes were used to develop the design method described in Chapter 6. While the third CMOS power amplifier was developed using this design method.

8.1 The First CMOS Power Amplifier

The first CMOS power amplifier was a low-risk design primarily suited to obtain valuable information about modeling and simulation of power amplifiers. Another goal of the power amplifier was to investigate stability problems and output matching topologies.

To limit the number of problems the operating frequency was 900 MHz, corresponding to the GSM-900 standard. Besides the complete power amplifier the individual amplifying stages were available for testing on the die. The on-chip biasing network was limited to the RF parts with the DC part placed off-chip.

8.1.1 Specifications

As mentioned above the first CMOS prototype was targeted towards the GSM-900 standard. The most important specifications for the power amplifier are listed in Table 8.1.

Table 8.1 Specifications for the first CMOS PA prototype.

Parameter	Min.	Nom.	Max.	Unit
Input freq.	880		920	MHz
Input power level	5		10	dBm
Max. output power	34.5			dBm
Input impedance		50		Ohm
Output impedance		50		Ohm
Power added efficiency	40			%

8.1.2 Packaging

The packaging of the IC plays an important role in the design of a power amplifier. The parasitics of the package, i.e. inductance and capacitance, has a big influence on the matching networks of the power amplifier. Another issue with packaging for power amplifiers is the thermal conduction, since the power amplifier produces a lot of excess power.

A solution which is relatively easy to model and has good thermal conduction is the chip-on-board approach. The principle in chip-on-board is simply to glue the die directly onto the PCB. The pads of the IC are then wire-bonded directly onto the PCB wires. In order to be able the bond reliably, the PCB must be plated with minimum 7 μm gold. The properties of chip-on-board resembles the properties of the ceramic substrates widely used for commercial power amplifiers without passive integration in the board,

but at a lower cost. The chip-on-board approach was therefore chosen for the CMOS prototypes.

8.1.3 Design of the Power Amplifier

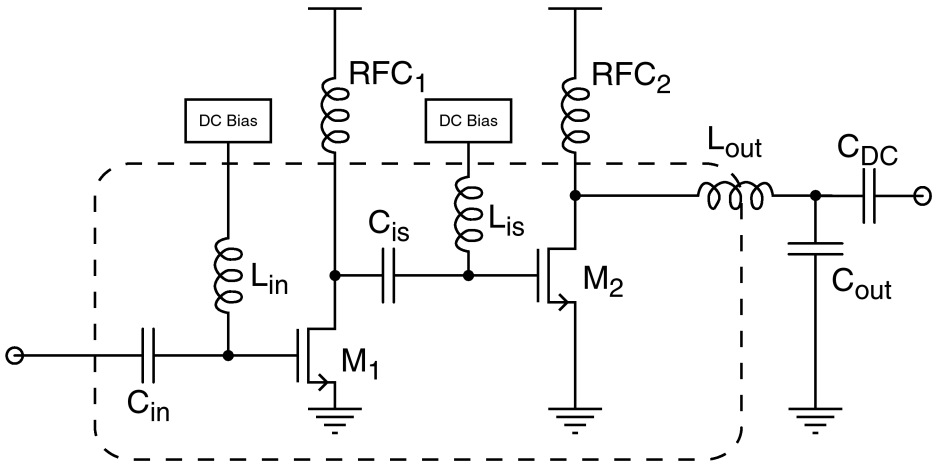

Figure 8.1 Schematic of the first CMOS power amplifier prototype.

The power amplifier consists of two stages with fully integrated input and interstage impedance matching networks. The schematic of the power amplifier is shown in Figure 8.1. The input matching network transforms the conjugate gate impedance Γ_{IN} to 50Ω as well as cancel the effect of the bondwires. It is made of a fully integrated highpass LC matching section. This has been chosen because it incorporates DC blocking and biasing at the same time as the impedance matching. The inductor is a spiral inductor implemented in top metal layer, while the capacitor is a thin-oxide plate capacitor between the two lowest metal layers.

The input stage operates in class AB, delivering up to 15 dB gain at maximum output power. The transistor of the input stage is 1 mm wide and 0.35 μm long. The input stage has an off-chip inductor acting as a RF choke (RFC).

The interstage matching network consists of a LC highpass section for the same reasons as the input matching network. The implementation is made in the same way as the input matching, but the interstage matching transforms the gate impedance to the desired output load of the input stage.

The output stage operates in class AB close to B. There are a number of reasons to choose this mode of operation:

1. Class AB close to B behaves relatively linearly. This is not the case for class C and E amplifiers. The performance is, however, not as good as class A.
2. The efficiency is relatively good, the theoretical maximum is 78.5%, compared with 50% for the class A amplifiers, class C and E have theoretical efficiencies up to 100%.
3. The maximum drain voltage is twice the supply voltage, this is important due to the possible breakdown of the gate-oxide. Class C and E amplifiers easily exceed three times the supply voltage.

4. The power utilization factor (PUF), which is a measure of the gain compared to the output power, is reasonable compared to class A, and better than class C and E.
5. The required output load is not too low to implement efficiently, which is often the case for class C.

The output transistor is 8 mm wide and has a length of 0.35 μm as the input stage. The transistor is partitioned into 6 separate finger transistors, with 30 fingers each. The gain of the output stage is approximately 12 dB.

The output matching network is placed off-chip due to efficiency considerations. The RFC for the output stage is an SMD mounted inductor. The output matching network consists of a bandpass T section, with a high transformation factor from approximately 4 Ω to 50 Ω. In the design of the network, the parasitics of the RFC microstrip were included.

In the design phase the two amplifier stages were initially treated separately and optimized for 50 Ω input and output matching using load-pull simulations. After each stage had been optimized an interstage matching network was designed using the impedances found for each stage.

8.1.4 Measurements

As explained above, the CMOS power amplifier IC has been mounted on an ordinary gold-plated PCB, and connected with wirebonding from the IC directly to the PCB. This approach offers some advantages during the prototyping phase of the design. The PCB can be produced with a PCB milling machine or at a normal PCB production facility. A new test-board can be milled within hours, allowing for larger exploration of the design space in the prototyping phase. There are however also some drawbacks when milling the PCB, most importantly it is not possible to make filled via holes. The via holes will then have to be filled with a wire and soldered on both sides of the PCB. The dielectric material used for the PCB was standard FR4, with a relative dielectric constant of approximately 4.3 at 1.75 GHz.

The output power and efficiency of the power amplifier over the desired frequency range has been depicted in Figure 8.3. One of the most important aspects of the reliable design of a power amplifier is accurate simulations. As mentioned above a lot of emphasis was put on accurate simulations. The simulated and measured data was compared, and minor modelling problems fixed, resulting in simulations with good agreement between simulated and measured results.

8.1.5 Summary of First CMOS Power Amplifier

A CMOS power amplifier has been presented with an output power of 28.8 dBm. The power added efficiency of the complete power amplifier is 35%. The operating frequency of the amplifier is 860-900 MHz, which is 20 MHz lower than expected but still reasonably close. Simulations show that a new PCB would improve both output

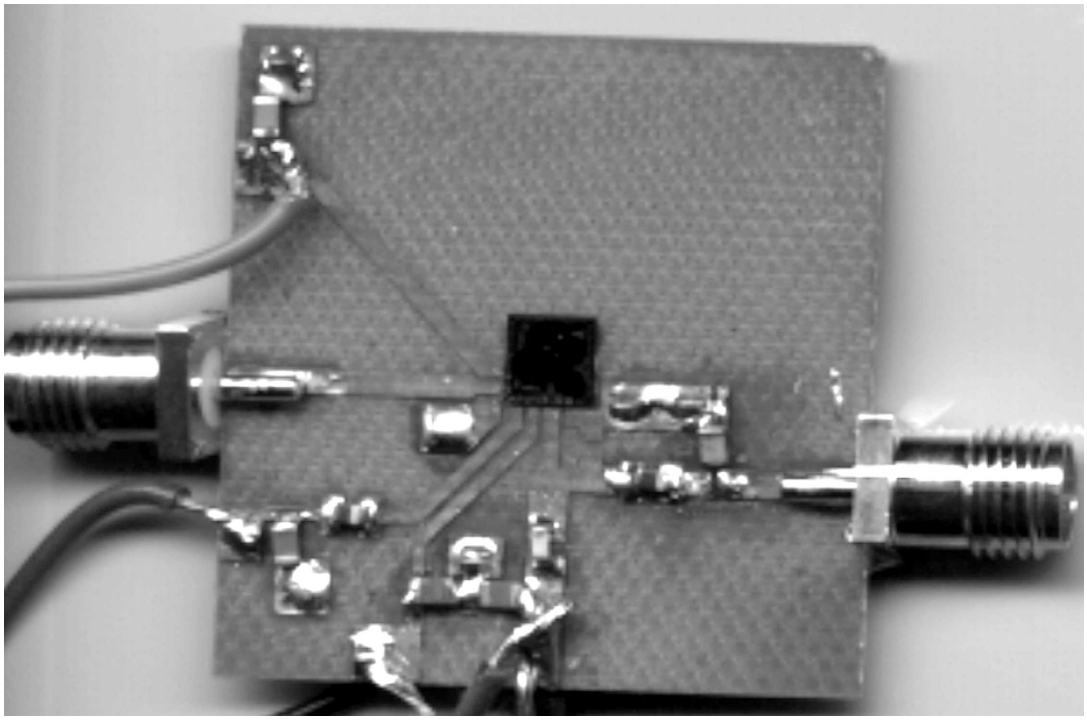

Figure 8.2 Photograph of the first CMOS power amplifier PCB.

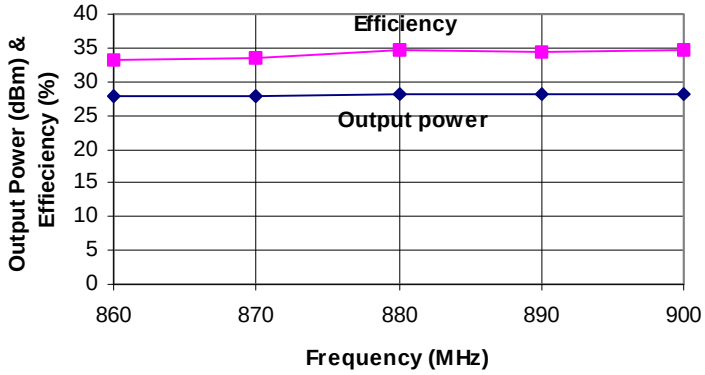

Figure 8.3 Output power and power added efficiency of first CMOS PA.

power and efficiency of the power amplifier. The die area including pads is 2.5 sq. mm. The tolerances in the bondwires were too big, therefore the next version contains on-chip decoupling capacitors, to establish RF ground on-chip.

Based on the measurements, the modeling of the power amplifier was improved, and used in the circuit simulator. Using the new model the simulation accuracy improved. Simulations showed that moving part of the output matching network on-chip, would greatly improve the output power and efficiency, since second harmonic termination becomes more effective. The basic properties of the power amplifier have been outlined in Table 8.2.

Table 8.2 Characteristics of the first CMOS power amplifier.

Process	0.35 μm CMOS
Supply voltage	3.5 V
Input power	5 dBm
Output power	28.8 dBm
Frequency	860-900 MHz
Power added efficiency	35%
Die area	1.9 sq. mm.

8.2 The Second CMOS Power Amplifier

Based on the experiences from the first CMOS prototype a second version was designed. The process and packaging are the same as for the first CMOS prototype. The second version featured an improved pad and output transistor layout. The bias signals were decoupled on-chip in order to control the center frequencies of the matching networks.

8.2.1 Specifications

The second CMOS power amplifier was targeted towards the GSM-1800 standard. The specifications for the power amplifier are listed in Table 8.3.

Table 8.3 Specifications for the second CMOS PA prototype.

Parameter	Min.	Nom.	Max.	Unit
Input freq.	1710		1785	MHz
Input power level	5		10	dBm
Max. output power	31.5			dBm
Input impedance		50		Ohm
Output impedance		50		Ohm
Power added efficiency	40			%

8.2.2 Design of the Power Amplifier

Compared to the first CMOS power amplifier a number of problems identified were corrected in the second version. In the second version the pads were placed better with regards to bonding. The layout of the output transistor was improved. The bias points were decoupled on-chip to achieve lower sensitivity to the bondwires.

In order to have better harmonic termination, a capacitor is placed on-chip, directly at the drain of the transistor, in parallel with the drain-source capacitor of the transistor. This capacitor terminates the harmonics at the drain, but at the same time it transforms the output impedance even lower, leaving a more difficult matching problem [1]. The RFC for the output stage is a relatively short microstrip which can be implemented without increasing the PCB size.

8.2.3 Simulations

In order to make precise simulations the PCB was characterized using simple short, open and through structures. Using this approach, the transients in the SMA connector to PCB interface could be modeled accurately. The simulations of these test structures showed very good agreement with measured results up to 4 GHz. After the SMA connectors and PCB were characterized, the output matching network was simulated and measured.

The PCB has been modeled with microstrip lines and the SMD components have been modeled according to vendor specifications. The bondwires have been modeled as inductors and the mutual coupling between the bondwires were included as well.

The measurements of the output matching network were performed by mounting a short piece of semi-rigid cable in place of the IC. The shield of the cable was soldered to the ground plane, where the IC was supposed to be placed. The conductor of the cable was attached at the microstrip on the PCB where the bondwires from the output of the IC would go.

The IC simulations were based on parasitic extraction results from the transistor and passive layout. The transistors were modeled by the MOS9 model. The spiral inductors and the metal-metal capacitors were simulated using lumped models delivered by the foundry.

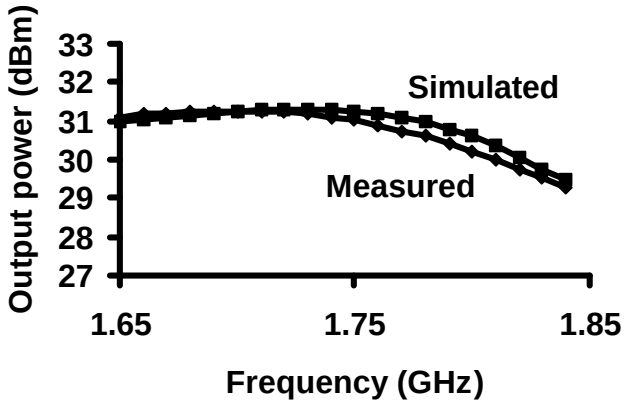

Figure 8.4 Comparison of simulated and measured data.

The simulations were made in the APLAC simulator, primarily with small-signal and harmonic balance simulations. For verification purposes transient simulations have been performed in the Eldo simulator. The harmonic balance simulations proved to be faster than the transient simulations, since only the steady-state solution is calculated, the precision of the simulations proved to be the same.

The simulations of the complete power amplifier including the PCB showed very good agreement between the simulated and measured results. The measured output power was predicted within a few tenths of a dB. The comparison between simulated and measured output power is shown in Figure 8.4.

8.2.4 Measurements

To get a realistic picture of the performance, the measurements were made in pulsed mode according to the GSM1800 specifications, this means a duty cycle of 12.5%. The measurements showed that the input matching network was matched 70 MHz too high. The interstage matching network on the other hand was matched 80 MHz too low. This means that the maximum output power was obtained at 1670 MHz instead of the desired center frequency of 1750 MHz. Another effect of the mistuned matching networks was that the input power had to be increased to get maximum output power and efficiency. The highest power added efficiency was 40% at 1730 MHz, with an output power of 30.3 dBm. The output power and efficiency biased for maximum power added efficiency vs. frequency is shown in Figure 8.6.

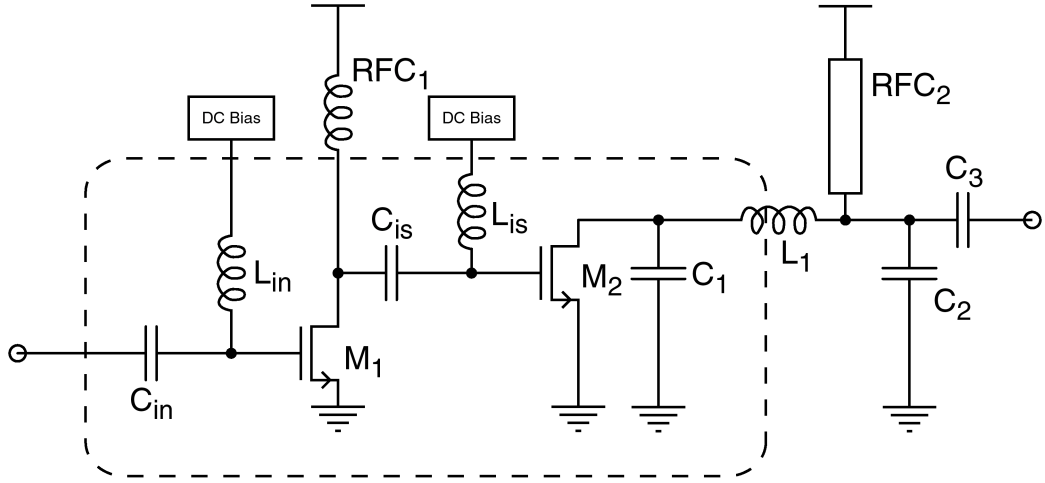

Figure 8.5 Schematic of the second CMOS power amplifier.

The highest output power obtained was 31.5 dBm at 1670 MHz, with the input power increased to 15 dBm. The output power and efficiency with biases set for maximum output power vs. frequency is shown in Figure 8.7

In spite of the problems with the matching networks it was still possible to get 30.3 dBm output power with a power added efficiency of 40% at 1730 MHz. With minor adjustments of the matching networks a new version of the IC can be designed to get the highest output power and efficiency in the GSM-1800 band, while keeping the input at the desired 5 dBm.

Since the power amplifier is operating in class AB close to B, it is inherently more linear, than e.g. the class C, D and E amplifiers demonstrated in CMOS so far [2][3][4][5]. This means that the power amplifier is suitable for digital predistortion as described in [6] and [7]. In [6] it was shown, that an improvement of the adjacent channel power ratio (ACPR) of 4-6 dB, is possible with simple low-power digital predistortion. This again means that class AB power amplifiers can be used in most upcoming amplitude modulated systems.

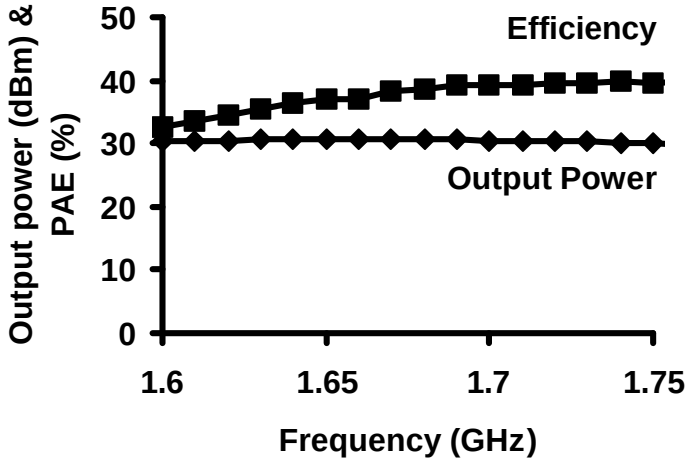

Figure 8.6 Measured output power and efficiency, biased for maximum power added efficiency.

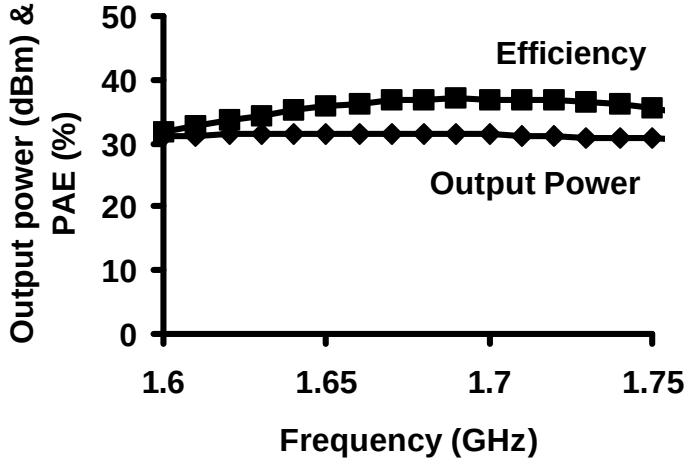

Figure 8.7 Measured output power and efficiency, biased for maximum output power.

The power amplifier operates on a supply voltage from 1 V to 3.6 V. The output power and efficiency vs. supply voltage is shown in Figure 8.8. The maximum output power was measured to be 32.2 dBm at 3.6 V.

One of the most important aspects of the reliable design of a power amplifier is accurate simulations. As mentioned above a lot of emphasis was put on accurate simulations. The simulated and measured data was compared, minor modeling problems fixed, and good agreement between the simulated and measured results were obtained.

8.2.5 Revised PCB Version

Once the simulations were accurate it was possible to start optimizing the PCB layout based on the simulations. After investigating a number of options it was clear that the inductor used as the RF choke on the output stage contributed significantly to the

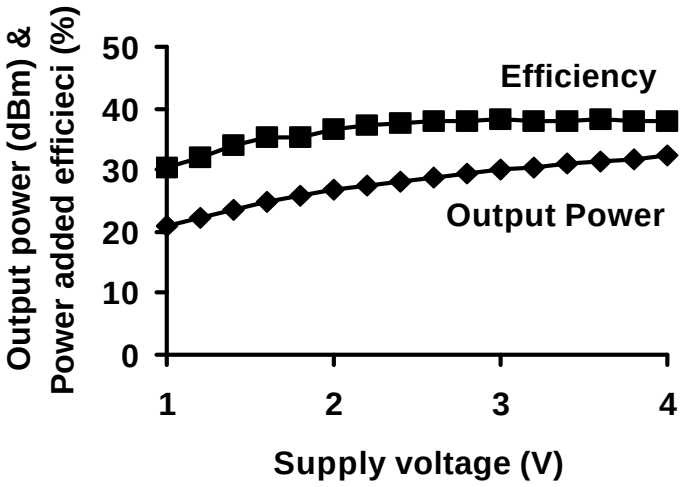

Figure 8.8 Measured output power and efficiency vs. supply voltage.

losses. The simulations showed that replacing the inductor with a short microstripline would increase the power added efficiency to 45%.

A new PCB was milled and a new set of measurements were performed. The measurements performed showed very good agreement with the results predicted by the simulations.

The highest power added efficiency was 45% at 1730 MHz, with an output power of 30.4 dBm. The output power and efficiency measurements with the power amplifier biased for maximum power added efficiency vs. frequency are shown in Figure 8.9.

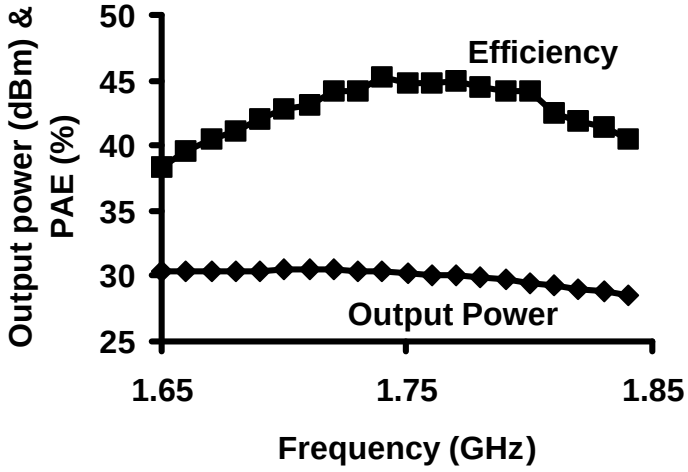

Figure 8.9 Output power and efficiency vs. frequency, biased for maximum efficiency

The highest output power obtained was 31.3 dBm at 1720 MHz. The output power and efficiency measurements with biases set for maximum output power vs. frequency are shown in Figure 8.10.

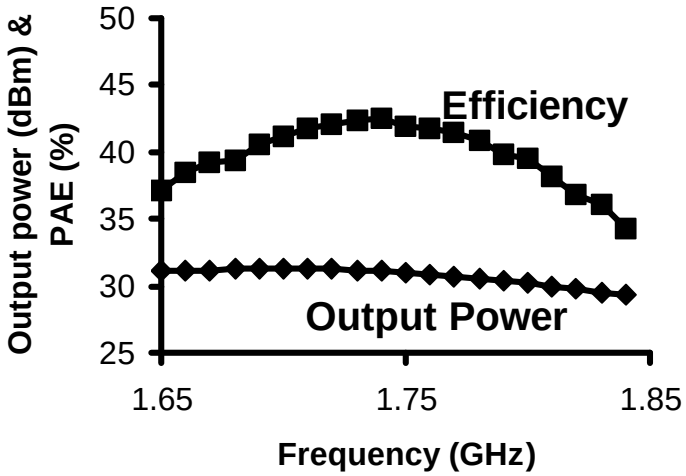

Figure 8.10 Output power and efficiency vs. frequency, biased for maximum output power

The power amplifier operates on a supply voltage from 1 V to 3.6 V. The output power and efficiency vs. supply voltage is shown in Figure 8.11.

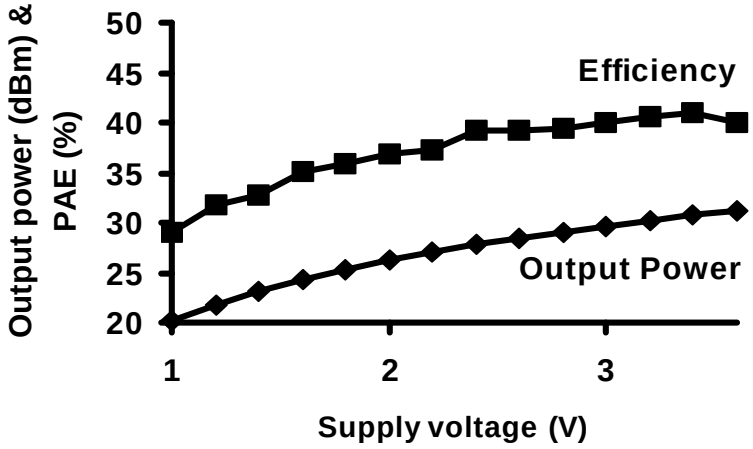

Figure 8.11 Measured output power and efficiency vs. supply voltage at 1730 MHz.

8.2.6 Summary of Second CMOS Power Amplifier

A CMOS power amplifier has been presented with an output power of 31.3 dBm at 1720 MHz. The power added efficiency for the complete power amplifier is 45% achieved at 1730 MHz. A redesign with minor adjustments of the input and interstage matching networks will move maximum output power and efficiency to the GSM-1800 band.The die area including pads is 1.9 sq. mm. The values of the components are listed in Table 8.4.

Based on the measurements, the modeling topology has been improved, and used in the circuit simulator. Using the new topology the simulation accuracy was improved, and is now within a few tenths of a dB, compared to measured results. The methods used to achieve this accuracy have been described in Chapter 5. The transistor model was a

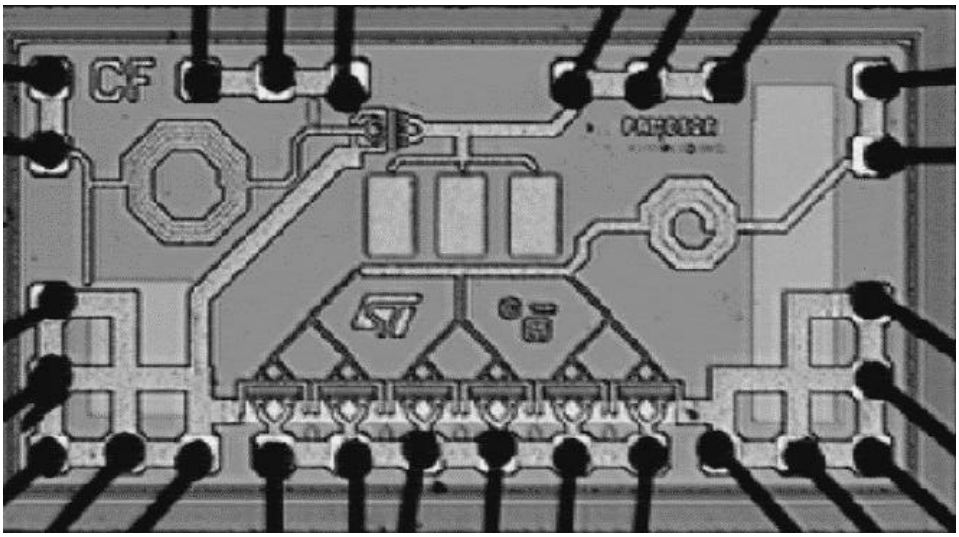

Figure 8.12 Photograph of the IC.

Table 8.4 Component values for the second CMOS power amplifier

Component	Value
Cin	0.8 pF
Lin	5.5 nH
Cis	50.0 pF
Lis	1.05 nH
C1	5.0 pF
L1	parasitic
C2	4.7 pF
C3	9.4 pF
RFC1	5.1 nH
RFC2	13.0/1.0 mm
M1	1000.0/0.35 µm
M2	6x1333.3/0.35 µm

MOS9 model with the enhancements described in Section 5.3.5. The passive components, the package and the PCB were modeled as described in Section 5.4.

The power amplifier consists of one die, two RFCs and three matching component plus decoupling capacitors, compared to 3 dies and 15-20 passives plus decoupling capacitors for a typical commercial GaAs power amplifier were the integration level is typically low.

The power amplifier operates in class AB, which gives good output power, efficiency and linearity. Until now no 1 W CMOS power amplifiers, which do not operate in a switched mode, have been published. The fact that this power amplifier operates relatively linearly, means that it is easier to use in wireless applications, especially in systems which utilizes amplitude modulation, such as IS-95, EDGE and

WB-CDMA. The basic properties of the power amplifier have been outlined in Table 8.5.

Table 8.5 Characteristics of the second CMOS power amplifier.

Process	0.35 μm CMOS
Supply voltage	3.5 V
Input power	5-15 dBm
Output power	31.5 dBm
Frequency	1710-1785 MHz
Power added efficiency	45%
Die area	1.9 sq. mm.

8.3 Third Revision CMOS Power Amplifier

The third revision CMOS PA is an improvement of the second CMOS PA, which contains integrated bias circuitry and improved performance of the on-chip matching networks. The features that were considered for the third revision of the power amplifier were on-chip RFC for first stage and on-chip output matching to approximately 10Ω. These changes did not make onto the chip due to lack of time. These possible features would only affect the integration level of the PA, reducing the external component count to two plus decoupling.

Compared to the second CMOS power amplifier the on-chip input and interstage matching networks were fine-tuned based on more precise active and passive models from the foundry. A simple resistive bias network was implemented on-chip with all necessary decoupling capacitors. This means that no external components were needed off-chip for the biasing.

The layout of especially the output transistor was improved to reduce the ground inductance. Even more ground bonds were added also to reduce the ground inductance. Furthermore the groundplanes of the first and second stage of the power amplifier were separated.

The PCB was produced at a commercial facility to get better vias. On the PCB two short microstrips were used in place of the RFCs. In general the ground plane on the PCB was vastly improved.

At last the use of the design method described in Chapter 6 also lead to some improvements. Especially the use of the simulated load-pull was very useful.

8.3.1 Design

The design of this power amplifier followed the design and simulation methodologies described in Chapter 6. The first choice to make was the number of stages in the power amplifier. In this case a two-stage methodology was chosen.

Then the class of operation was chosen for each of the stages. The input and output stages operates in class AB close to class B. The reasons for choosing class AB operation are the same as those outlined in Section 8.1.3.

Once the class of operation was chosen for the output stage it was possible to start the dimensioning of the output transistor. This dimensioning was an iterative process where the initial guess originated from the I-V characteristic of the output transistor. From the I-V characteristic it was possible to find the voltage and current swings possible for a given load-line. From the voltage and current swings the maximum output power was then determined and a reasonable size of the transistor was found.

After an initial value is selected the more accurate RF behavior is found using load-pull simulations. The load-pull simulations are the simulation equivalent of the load-pull measurements as described in Section 3.2.3. The output from the load-pull simulations are shown in Figure 8.13. Two sets of contours are presented in the figure namely output power shown in black with the center and 1, 2 and 3dB contours. The power added efficiency in grey shows center 5, 10 and 15% contours. The load-pull simulation was used to make the trade-off between output power and power added efficiency. The selected load impedance is approximately *4-j4*Ω.

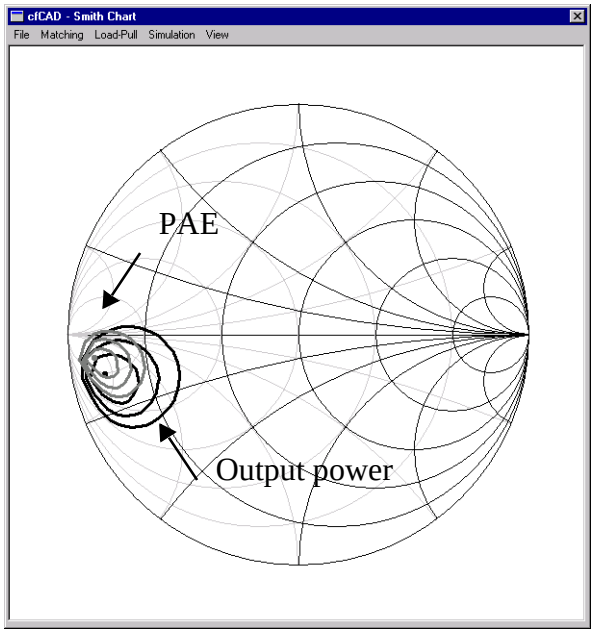

Figure 8.13 Load-pull simulation of third CMOS power amplifier.

The final schematic of the power amplifier is shown in Figure 8.14 where the components mentioned below can be located. The output transistor (M_2) was then chosen to be 8 mm wide and with a length of 0.35 µm. The transistor is partitioned into 6 separate finger transistors, with 70 fingers each. The input stage also operates in class AB. The transistor of the input stage (M_1) is 1 mm wide and 0.35 µm long.

The output matching network is placed primarily off-chip due to efficiency considerations. In order to have better harmonic termination, a capacitor (C_1) is placed on-chip, directly at the drain of the transistor, in parallel with the drain-source capacitor

of the transistor. This capacitor terminates the harmonics at the drain, but at the same time it transforms the output impedance even lower, leaving a more difficult matching problem. The RF chokes (RFC_1, RFC_2) for the output stage as well as the input stage are relatively short microstrips, which can be implemented without increasing the overall PCB size. The output matching network consists of a bandpass T section (L_1, C_2, C_3), due to the high transformation factor from 4 Ω to 50 Ω. The choice of the T section gives a larger bandwidth than a single L section. The inductor in the T section consists of a contribution from the bondwires as well as from the microstrip. In the design of the network, the parasitics of the RFC microstrip were also included.

The input and interstage matching networks were both made with a fully integrated highpass LC matching section. This was chosen because it incorporates DC blocking and biasing at the same time as the impedance matching. The on-chip inductors are spiral inductors implemented in the top metal layer, while the capacitors are made thin-oxide metal-metal capacitors in the two lowest metal layers.

The schematic of the third CMOS power amplifiers is shown in Figure 8.14. The

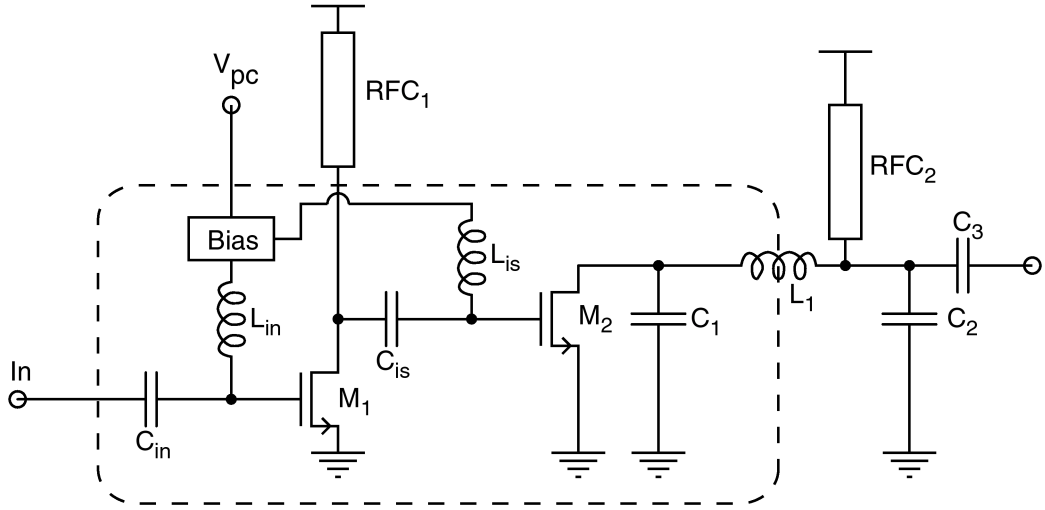

Figure 8.14 Schematic of third CMOS power amplifier.

components and their values are listed in Table 8.6. Further details on the design of the power amplifier can be found in Appendix A.

8.3.2 Measurements

The CMOS power amplifier IC was mounted directly on the PCB and wire bonded directly onto the PCB microstrips as was the case with the other CMOS power amplifiers. The PCB for this power amplifier was produced at a normal PCB production facility and the PCB was the gold plated with 7μm gold. This meant that good filled via holes were available hence improving the effectiveness of the groundplane on the PCB.

The passive components used on the PCB were 0402 SMD components. The SMA connectors were mounted horizontally on the edge of the PCB, in order to reduce the

effects of the transition from SMA connector to PCB microstrip. The die photo is shown in Figure 8.15 while the PCB is shown in Figure 8.16.

Table 8.6 Component values for third CMOS power amplifier

Component	Value
Cin	1.0 pF
Lin	3.9 nH
Cis	20.0 pF
Lis	1.4 nH
C1	5.0 pF
L1	parasitic
C2	4.7 pF
C3	3.9 pF
RFC1	10.0/0.25 mm
RFC2	10.0/0.25 mm
M1	1000.0/0.35 µm
M2	6x1333.3/0.35 µm

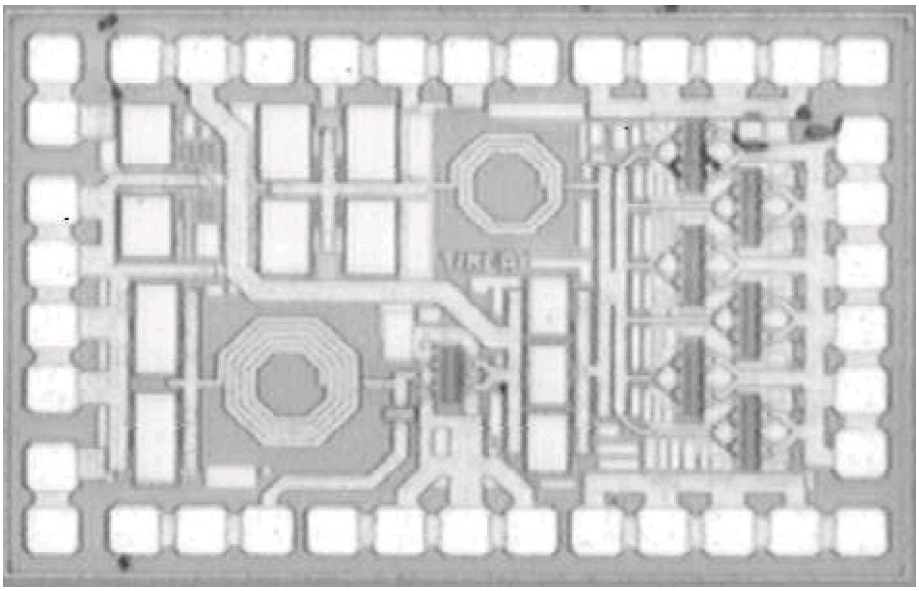

Figure 8.15 Die photograph.

To get a realistic picture of the performance, the measurements were made in pulsed mode according to the GSM1800 specifications, this means a duty cycle of 12.5%.

The highest power added efficiency was 55% at 1750 MHz, with an output power of 30.4 dBm. The output power and efficiency measurements with the power amplifier biased for maximum power added efficiency vs. frequency are shown in Figure 8.17. The power added efficiency stays above 50% from the start of the measurements at 1.65GHz to 1.83GHz. While the output power starts at 30.8dBm at 1.65 GHz and stays above 30dBm till 1780 MHz.

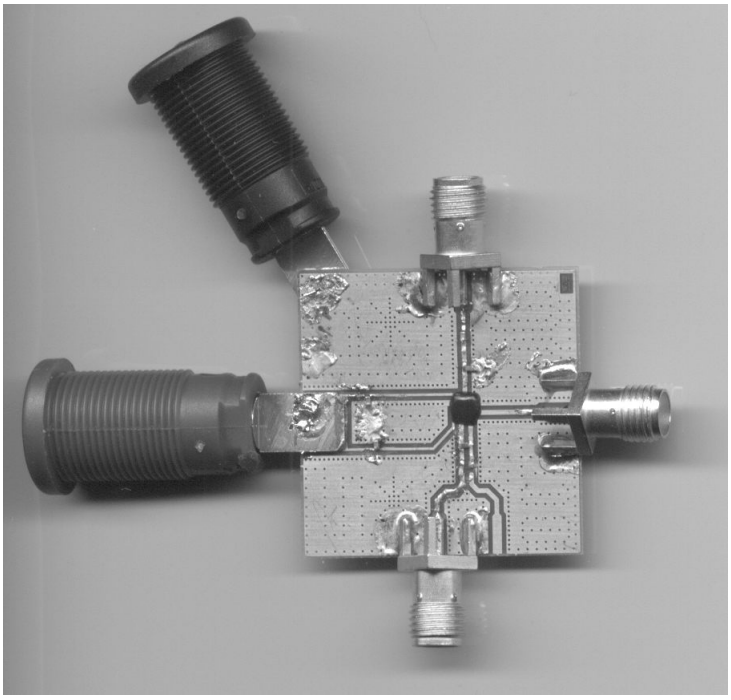

Figure 8.16 PCB photograph.

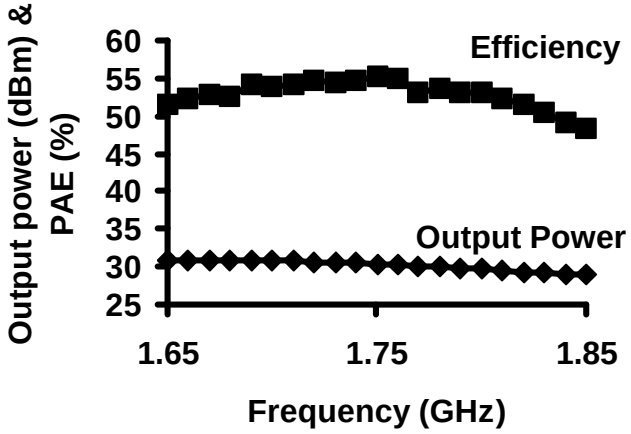

Figure 8.17 Output power and power added efficiency vs. frequency when biased for efficiency.

The power amplifier operates on a supply voltage from 1 V to 3.4 V. The output power and efficiency vs. supply voltage is shown in Figure 8.18. The output power is 20.8 dBm at 1V and 31.4 dBm at 3.4 V. The power added efficiency varies from 43% to 55% at 1V and 3.4V respectively. The power amplifier did not have sufficient attenuation to be a plug-in for a standard mobile phone but this could easily be achieved using a third stage between the first and second stages. Apart from the missing attenuation the power amplifier was able to fulfill the requirements of the power-ramp mask in GSM.

A comparison of all the published CMOS power amplifier results is shown in Table 8.7. As can be seen from the table no other CMOS power amplifier has been

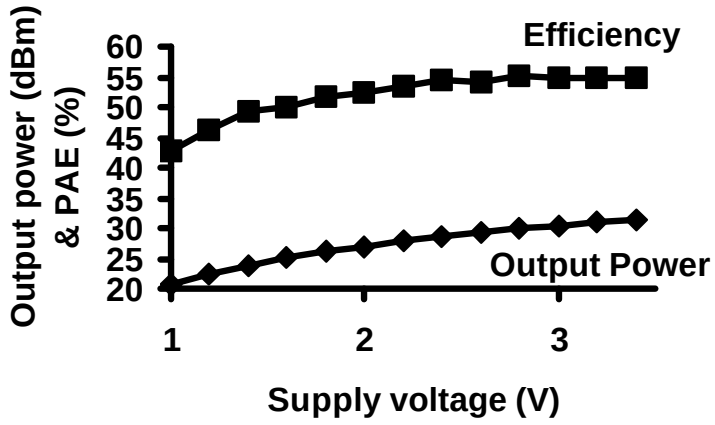

Figure 8.18 Measured output power and power added efficiency vs. supply voltage at 1750 MHz.

published with output power or power added efficiency as high as the work presented here.

The simulations for the complete power amplifier including the PCB showed very good agreement between the simulated and measured results. The measured output power was predicted within a few tenths of a dB. The efficiency deviated less than 1%. The comparison between simulated and measured output power is shown in Figure 8.19.

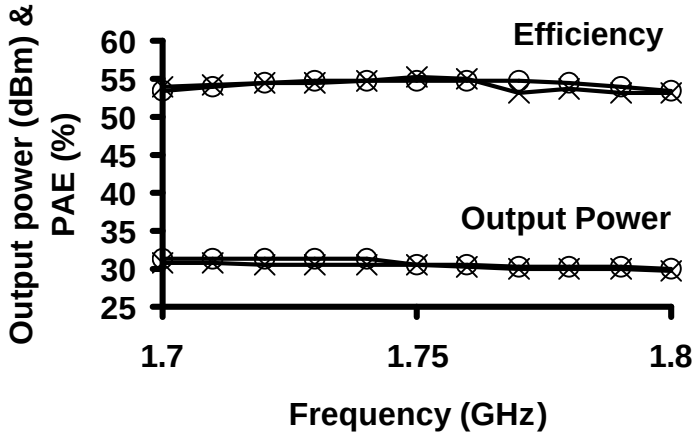

Figure 8.19 Comparison of simulated and measured data.

8.3.3 Summary of Third CMOS Power Amplifier

A CMOS power amplifier has been presented with a power added efficiency of 55% with an output power of 30.4 dBm at 1750 MHz. The power amplifier is designed for GSM-1800 with a supply voltage of 3V, although it performs very well from 1V to 3.4V. The die area including pads is 1.1 sq. mm. By accurately modeling bondwires, microstrips and SMD components the accuracy of the simulations was within a few tenths of a dB, compared to measured results.

The power amplifier consists of one die, two short microstrips and two matching components plus decoupling capacitors, compared to 3 dice and 15-20 passives plus decoupling capacitors for a typical GaAs power amplifier. The power amplifier has higher power added efficiency than any other CMOS power amplifier results published so far, whether they operate linearly [8][9][10]*[11]* or nonlinearly [12][2][13][5]. This

Table 8.7 Comparison of CMOS power amplifiers.

	Frequency (MHz)	**P_{out} (dBm)**	**PAE (%)**	**Class**
T. Melly et. al. [12]	430	4.0	15	C
S.-J. Yoo et. al. [8]	433	13.0	30	AB
D. Su et. al. [2]	830	30.0	42	D
Fallesen (Section 8.1)	*880*	*28.8*	*35*	*AB*
B. Ballweber et. al. [9]	900	19.3	23	AB
C. Yoo et. al. [13]	900	29.5	41	E
K.-C. Tsai et. al. [5]	1980	30.0	41	E
Asbeck et. al. [10]	1950	29.2	27	B
Fallesen et. al. [11]	*1730*	*30.4*	*45*	*AB*
Fallesen et. al. [14]	***1750***	***30.4***	***55***	***AB***

work will be presented in *[14]*.

The basic properties of the power amplifier have been outlined in Table 8.8.

Table 8.8 Characteristics of the third CMOS power amplifier.

Process	0.35 μm CMOS
Supply voltage	3.0 V
Input power	5 dBm
Output power	31.3 dBm
Frequency	1710-1785 MHz
Power added efficiency	55%
Die area	1.9 sq. mm.

8.4 Summary

The first CMOS power amplifier prototype was representative for the CMOS power amplifiers presented at the time of the measurements. The two last CMOS power amplifiers were however better than all other work published at the time of publication. The second power amplifier is on the same level as the other CMOS power amplifiers presented so far, while the third power amplifier has significantly better power added efficiency than any other CMOS power amplifier.

The good experimental results have been obtained by working structured through the entire design process. The very first experiments were done using a discrete LDMOS transistor in a discrete single stage power amplifier. This initial design revealed a number of the potential problems especially stability problems. In the first CMOS power amplifier design special focus was placed on stability and simplicity. This meant that the bias networks were placed off-chip and the two stages were also available in single stage versions.

The first CMOS power amplifier exposed a number of problems, especially in the areas of bias stability and layout. In the second CMOS power amplifier these problems were corrected and the operating frequency was changed from GSM-900 to GSM-1800. The second power amplifier behaved close to the simulated performance, but some of the parasitic components were not estimated accurately, resulting in a slightly lower operating frequency than expected. The second CMOS power amplifier was used to obtain detailed information of what parameters are important while designing and simulating an integrated power amplifier.

Using the experiences from the first two CMOS power amplifiers a design method was developed. This design method was used to design the third CMOS power amplifier. The detailed insight in modeling and simulation of power amplifiers was then used to optimize the third power amplifier to level at which no other CMOS power amplifiers have achieved yet. The third power amplifier also achieved very good stability and good thermal performance.

The good results were obtained by using the consistent design method described in Chapter 6 combined with very accurate modeling of the power amplifiers described in Chapter 5. Careful design of the different groundplanes and matching networks also played an important role. The CMOS process was a bulk substrate with 10-20Ω-cm resistivity which combined with thick top metal layer and metal-metal capacitors gave good passive components.

During the design phase the simulated load-pull with the proper matching network topology was used to achieve the high efficiency. If only ideal impedances were presented to the power amplifier during the load-pull simulation the frequency dependent behavior and the losses would not be modeled correctly. In conjunction with the possibility to size the transistor this method proven very powerful.

The evolution of the CMOS power amplifiers have been tracked in Table 8.9. Compared to other CMOS power the second CMOS power amplifier is comparable to other CMOS power amplifiers published, while the third CMOS power amplifier is better than any other CMOS power amplifier reported. The comparison of the CMOS power amplifiers was shown in Table 8.7.

Table 8.9 Evolution of CMOS power amplifiers.

	First PA	Second PA	Third PA	
Center frequency	880	1730	1750	MHz
Output power	28.8	30.3	30.4	dBm
Power added efficiency	35	45	55	%
Die size	2.4	1.9	1.1	mm^2
External components	11	10	4	
Supply Voltage	3.3	3.5	3.0	V

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[2] D. Su and W. McFarland, "A 2.5-V, 1-W monolithic CMOS RF power amplifier," in *IEEE 1997 Custom Integrated Circuit Conference*, 1997.

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[5] K.-C. Tsai and P. R. Gray, "A 1.9 GHz 1-W CMOS class-E power amplifier for wireless communications," *IEEE Journal of Solid-State Circuits*, July 1999.

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[7] M. Ranjan, K. H. Koo, G. Hanington, C. Fallesen, and P. Asbeck, "Microwave power amplifiers with digitally-controlled power supply voltage for high efficiency and high linearity," in *2000 IEEE MTT-S International Microwave Symposium*, (Boston, USA), June 2000.

[8] S.-J. Yoo, H. J. Ahn, M. M. Hella, and M. Ismail, "The design of 433 MHz class AB CMOS power amplifier," in *2000 Soutwest Symposium on Mixed-Signal Design*, pp. 26--40, 2000.

[9] B. Ballweber, R. Gupta, and D. J. Allstot, "Fully-integrated CMOS RF amplifiers," in *International Solid-State Circuits Conference*, pp. 154--155, 1999.

[10] P. Asbeck and C. Fallesen, "A RF power amplifier in a digital CMOS process," in *18th NorChip Conference*, (Turku, Finland), November 2000.

[11] C. Fallesen and P. Asbeck, "A 1 W 0.35 um CMOS power amplifier for GSM-1800 with 45% PAE," in *2001 IEEE International Solid-State Circuits Conference*, (San Francisco, USA), February 2001.

[12] T. Melly, A.-S. Porret, C. C. Enz, M. Kayal, and E. Vittoz, "A 1.2V, 430 MHz, 4 dBm power amplifier and a 250uW front-end, using a standard digital CMOS process," in *1999 International Conference on Low Power Electronics and Design*, pp. 233--237, 1999.

[13] C. Yoo and Q. Huang, "A common-gate switched, 0.9W class-E power amplifier with 41% PAE in 0.2 um CMOS," in *2000 Symposium on VLSI Circuits*, pp. 56--57, 2000.

[14] C. Fallesen and P. Asbeck, "A 1W CMOS power amplifier for GSM-1800 with 55% PAE," in *2001 IEEE International Microwave Symposium*, May 2001.

CHAPTER 9
CONCLUSION

The primary goals of this thesis has been to develop a design method for highly integrated power amplifiers as well as demonstrate the feasibility of submicron CMOS power amplifiers for wireless communications. These goals were reached by explaining the basic theory behind RF power amplifiers and through experimental results.

In the first part of the thesis the basic theory of power amplifiers was described. The different classes of operation were discussed and advantages and disadvantages of the classes were summarized. Then the selection of load and source impedances of a single-stage power amplifier with either small-signal or large-signal methods was introduced. The simulated load-pull technique was developed and used in conjunction with the impedance matching network synthesis which was also described. In the experimental part of the thesis the simulated load-pull technique proved to be very powerful. The different network topologies were compared and the synthesis of these networks was treated. After the initial design issues were covered the biasing of the power amplifier was discussed, followed by techniques used to ensure stability of the designed power amplifiers.

The fundamental characteristics of the CMOS technology was described with a focus on the parameters important for power amplifier design. This included a coverage of the breakdown mechanisms present in submicron CMOS processes. The other technologies available for power amplifiers were briefly compared to CMOS and the choice of CMOS for the experimental work was motivated.

Another important issue was the problems associated with modeling of power amplifiers. The problems of modeling the CMOS transistors were explained and different simulation models were compared. The modeling of the passive components of a power amplifier on-chip as well as off-chip was discussed along with the package and thermal models.

Based on the theory in the first part of the thesis along with the experiences from the work with the CMOS power amplifiers a design method for integrated power amplifiers was developed. The design method covers the design of an integrated power amplifier from design specifications to complete power amplifier.

A digital predistortion system was introduced which enables the use of nonlinear power amplifiers in linear modulation systems. As a starting point the power amplifier has to be relatively linear. The improvement in ACPR was shown to be in the range 6-8 dB. The linearization technique was demonstrated on a dynamic supply voltage power amplifier. In this configuration a standard power amplifier for IS-95 was modified with dynamic supply voltage which deteriorated the ACPR. Applying the digital predistortion meant that the total efficiency of the power amplifier was improved by 40%, while restoring the original ACPR performance.

Based on the theory in the first part of the thesis three CMOS power amplifiers were built. The first power amplifier was for the GSM-900 standard, and showed an output power of 28.8 dBm with a power added efficiency of 35%. The remaining two power amplifiers were designed for the GSM-1800 standard. The first of the GSM-1800 power amplifiers showed an output power of 30.3 dBm with a power added efficiency of 45%.

The last power amplifier had even higher integration than the first two power amplifiers, with complete integration of input and interstage matching networks as well as a fully integrated bias circuit. The power amplifier had an output power of 30.4 dBm with a power added efficiency of 55%, which is better than any other results reported for a CMOS power amplifier and comparable to the results of power amplifiers in better but also more expensive technologies such as GaAs HBT. The power amplifier was designed using the design method described in Chapter 6. Using the modeling techniques described in Chapter 5 it was possible to achieve very good agreement between simulated and measured results.

This work has demonstrated that it is possible to design power amplifiers in a CMOS process with sufficient output power and power added efficiency. The CMOS power amplifiers designed through the project shows that very high integration is possible in CMOS, which leads to a very low component cost. Furthermore it was demonstrated that design methods developed during the project can be used to design integrated power amplifiers with very good performance.

In the future more effort will have to be placed in the development of CMOS simulation models for RF usage. Also the modeling of some of the passive components will have to be improved, especially the on-chip inductors.

There is no doubt about the fact that CMOS will be the cheapest process technology available for a long time to come. It is therefore important that all components for high volume, low cost products such as mobile phones can be produced in CMOS. The power amplifier has been one of the few components which have not been integrated in CMOS with sufficiently high performance, but this work has clearly demonstrated the feasibility of CMOS power amplifiers for mobile phones.

Appendix A
Design Details

In this appendix the details of the design of the third CMOS power amplifier will be described. This appendix is meant as a supplement to the design described in Section 8.3 rather than a complete description of the design. The design follows the design method described in Chapter 6.

The main specifications for the power amplifier has been repeated in Table A.1. The specification of the output power is slightly lower than necessary in a mobile phone, but this was chosen to minimize the risk of the project. By choosing this slightly lower output power it was possible to maintain the transistor sizing from the second power amplifier.

Table A.1 Specifications for the third CMOS PA prototype.

Parameter	Min.	Nom.	Max.	Unit
Input freq.	1710		1785	MHz
Input power level	5		10	dBm
Max. output power	30			dBm
Input impedance		50		Ohm
Output impedance		50		Ohm
Power added efficiency	50			%

A.1 Initial Design Decisions

The power amplifier is targeted towards GSM-1800 which is a constant envelope standard. This means that the power amplifier will be operated in saturation to obtain high efficiency.

The first choice is the between differential or single-ended operation. Based on the problems with differential antennas described in Section 2.5 and differential to single-ended conversion it was decided to design a single-ended power amplifier.

The next decision is the number of stages of the power amplifier. A two stage design was selected, since it gives sufficient gain, demonstrates the important issues and still has a reasonable complexity.

The gain and efficiency budget for the power amplifier is outlined in Table A.2.

Table A.2 Gain and efficiency budget

Stage	Gain	PAE
1. stage	12	55%
2. stage	12	55%
Total	**24**	**50%**

A.2 Design Individual Stages

The design of the individual stages starts by selecting the class of operation. Due to the reasons outlined in Section 8.1.3 both of the stages are operating in class AB.

A.2.1 Transistor Sizing and Load Selection

The transistors initial size is based on the I-V characteristics of the transistor. To find the initial size the I-V characteristics of a 1mm wide transistor was extracted. The I-V characteristics are shown in Table A.1.

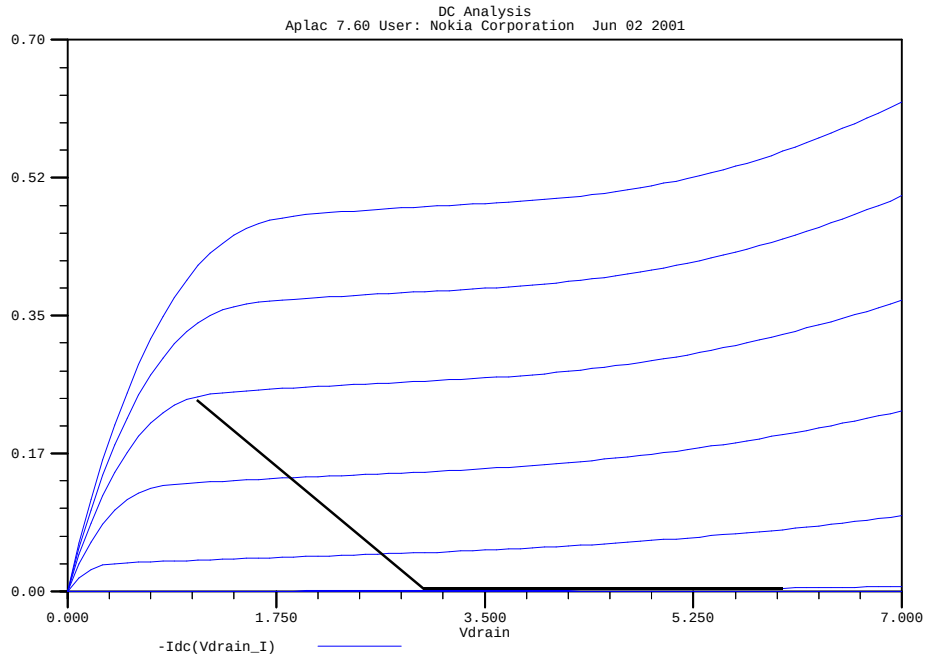

Figure A.1 I-V characteristics of 1mm wide transistor.

From the load-line drawn in the I-V characteristics an output power of 0.25W could be expected at low frequencies, since the operating frequency is 1.7GHz some headroom should be included.

The load-pull simulation results shown in Figure 8.13 was the result of an 8mm wide transistor with minimum channel length of 0.35μm. The trade-off between output power and efficiency was made by choosing the point on the 1dB power contour closest to maximum efficiency, this was approximately at *4-j4*Ω. The load-pull simulations included all the parasitics associated with the package and interconnects. Then the source impedance was found using the operating gain method described in Section 3.1.5. While the transistor size determines the maximum output power it does not have any direct influence on the efficiency of the power amplifier.

At last the output matching network was designed using the L matching section described in Section 3.3.3. Once the initial values were found the complete matching network including parasitics was simulated including RF choke and DC block. The network was then optimized using the simulator. The reason for choosing the simple L matching network is primarily to limit the losses in the matching network. Since the bandwidth of the power amplifier was sufficient this could not warrant the use of cascaded stages.

After the second stage had been designed the first stage was designed using the same methods. This resulted in a transistor width of 1mm and a synthesized input matching network. The input matching network was a simple L networks which allowed biasing.

To be able to make all these simulations accurately it has been necessary to employ the models described in Chapter 5. The transistor model used is MOS9 extracted by the foundry explicitly for RF purposes furthermore the RF extensions described in Section 5.3.5. The modeling of the passive components and package were done according to the models described in Section 5.4. Most interesting is probably the fact that a scalable inductor model was available directly from the foundry. The scalable inductor model is based on the model shown in Figure 5.5.

A.3 Combination of Stages

After the designing the two stages separately they had to be combined into a complete power amplifier. First the interstage matching network was designed based on the load impedance of the first stage and the source impedance of the second stage. The interstage matching network was a simple L section as was the case for the input matching of the first stage. Then the interstage matching network was optimized using simulations on the complete power amplifier.

After the interstage matching network had been optimized the RF performance of the complete power amplifier was verified. The output power and efficiency were simulated over frequency. The bias circuit is a couple of resistive voltage divider with ample decoupling capacitors. This circuit will not provide temperature compensation but shows the feasibility of on-chip bias circuits.

After the RF performance was verified the stability of the power amplifier was checked. The stability was checked as described in Chapter 4. All ports including bias ports were treated as RF ports and conventional small-signal stability theory was applied. Transient simulations were also used to verify the stability.

The voltage and current waveforms of the output transistor of the complete power amplifier are shown in Figure A.2. The dip in the current waveform is caused by the knee-effect and is one of the reasons for a reduced output power compared to the ideal I-V characteristics.

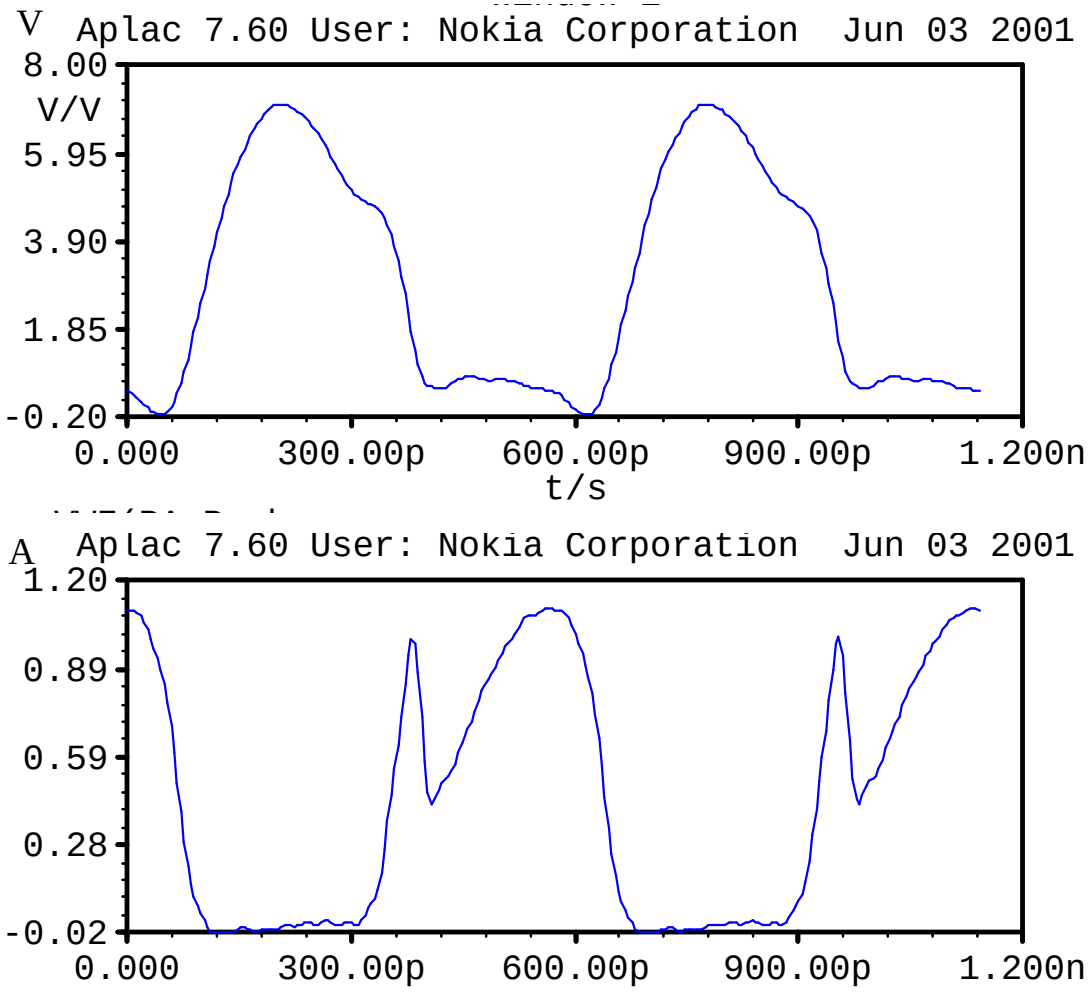

Figure A.2 Voltage across and current through the output transistor channel.

Appendix B
Published Papers

During the Ph.D. project a number of papers have been published. These papers are attached in this appendix. The references of the papers are listed below:

References

[1] C. Fallesen, G. Hanington, and P. M. Asbeck, "Improved linearity of a dynamic supply voltage power amplifier using digital predistortion," in *1999 IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, (San Diego, USA), September 1999.

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[7] P. Asbeck and C. Fallesen, "A RF power amplifier in a digital CMOS process," in *18th NorChip Conference*, (Turku, Finland), November 2000.

[8] P. Asbeck and C. Fallesen, "A polar linearisation system for RF power amplifiers," in *7th IEEE International Conference on Electronics, Circuits Systems*, (Kaslik, Lebanon), December 2000.

[9] P. Asbeck and C. Fallesen, "A 29dBm 1.9GHz class B power amplifier in a digital CMOS process," in *7th IEEE International Conference on Electronics, Circuits Systems*, (Kaslik, Lebanon), December 2000.

Improved Linearity of a Dynamic Supply Voltage Power Amplifier Using Digital Predistortion

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In the dynamic supply voltage (DSV) power amplifier, a dc-dc converter is used to adjust the power supply voltage provided to the output stage in accordance with the output signal level. This architecture can provide a significant increase in overall efficiency, particularly if the amplifier is operated at relatively low output power during a substantial fraction of the time [1,2]. It has been found, however, that the output linearity can be degraded in the DSV system. The reduced linearity results from a variation in amplifier gain as the supply voltage is varied. In previous work, it has been shown that by dynamically varying the gate bias in a MESFET-based DSV amplifier along with the power supply voltage (drain bias, VDD), the linearity of the amplifier can be restored [2]. In this work, we show that linearization of the DSV amplifier can also be easily performed by predistorting the signal fed to the amplifier, in a manner that can be accomplished with digital signal processing. Using a MESFET-based DSV amplifier, we show that DSP-based linearization allows the adjacent channel power ratio (ACPR) requirements of representative CDMA systems to be met.

The structure of the DSV amplifier (without linearization) is shown in fig.1. A dc-dc converter capable of rapid modulation (with a bandwidth comparable to that of the output signal bandwidth) is used to vary the supply voltage VDD over the range 3.4V to 10V, in accordance with the required drain voltage swing of the MESFET. Fig.2 illustrates the representative efficiency as a function of output power level obtained with a fixed VDD and a dynamically adjusted VDD. An improvement in overall efficiency of the amplifier can be calculated using the statistics of the output signal distribution. For representative cases, the improvement is near x1.4 [1]. Using the DSV technique, however, the amplifier gain G varies with input power level Pin in a manner typically shown in fig.3. In this work, we have introduced a digitally-computed fixed signal predistortion for an already existing DSP.

The distortion in the power amplifier can be modeled, to lowest order, using bandpass nonlinearity theory. The AM-AM and AM-PM characteristics of the amplifier are measured using CW single-tone signals, and used to model the amplifier output amplitude B(t) for modulated signals according to:

$$B(t) = G(A) \cdot e^{j\Phi(A)} \cdot A(t) \qquad (1)$$

where A(t) is the amplitude of the input signal, G(A) is the amplitude-dependent gain of the amplifier and $\Phi(A)$ is the amplitude-dependent phase contribution of the amplifier. The required predistortion is then the inverse function:

$$A_p(t) = 1/G_{dist}(A) \cdot e^{-j\Phi dist(A)} \cdot A(t) \qquad (2)$$

where G_{dist} is the deviation from the linear gain of the amplifier, and Φ_{dist} is the deviation from the linear phase contribution. For an efficient DSP implementation, it is necessary to do the predistortion at baseband, and operate separately on the I and Q signals. The equations for the predistorted I and Q signals are:

$$I_p = (I \cdot \cos \Phi_{dist} + Q \cdot \sin \Phi_{dist}) / G_{dist}(A), \; Q_p = (Q \cdot \cos \Phi_{dist} - I \cdot \sin \Phi_{dist}) / G_{dist}(A) \qquad (3)$$

In our implementation, the I and Q channels outputs were precomputed in software for a specific pseudorandom output data pattern, and fed to the system with a signal generator which allows arbitrary I and Q waveforms to be specified. The arbitrary waveforms can contain up to 1 Msample transferred to the signal generator through a GP-IB bus. The generation of the data is done using a C++ program. The digital predistortion presented here can be implemented very effectively in an already-existing DSP. The overhead for implementing the predistortion is six multiplications, one addition, one subtraction and 40-100 data entries in a table.

Measurements of the ACPR were done using a spectrum analyzer. A built-in function for the channel power calculation was used and the result was transferred to a computer and used for ACPR calculations. Averaging of results over many runs was done to obtain accurate values. Measurements have shown an improvement of the ACPR of the power amplifier described above on the order of 4-6 dB, as shown in fig.4. The output spectrum with or without predistortion is shown in fig. 5 and fig. 6. The resulting output spectrum is capable of meeting IS-95 requirements. The predistortion also means that the amplifier can be driven further into compression, thereby achieving a higher efficiency.

[1] G. Hanington, P. F. Chen, V. Radisic, T. Itoh, and P. M. Asbeck, "Microwave Power Amplifier Efficiency Improvement with a 10 Mhz HBT DC-DC Converter", *1998 IEEE MTT-S Intl. Microwave Symposium Digest*, **Vol. 2**, pp. 589-592 (1998).
[2] G. Hanington, P.F.Chen, L.Larson, K.Gard, and P. Asbeck (to be published)

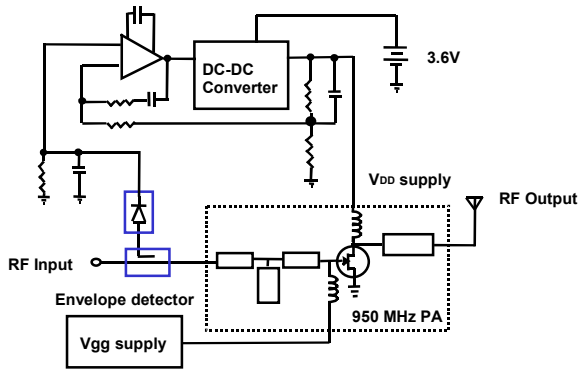

Figure 1: Dynamic supply voltage power amplifier

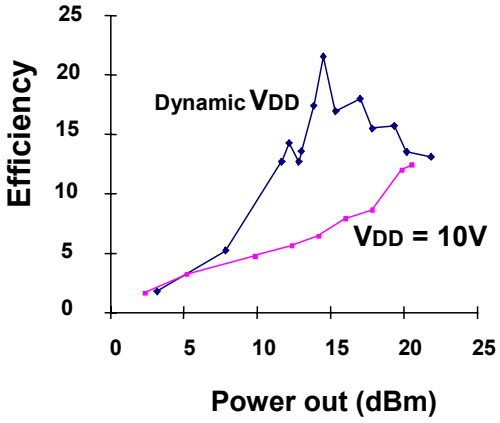

Figure 2: Total efficiency of DSV amplifier

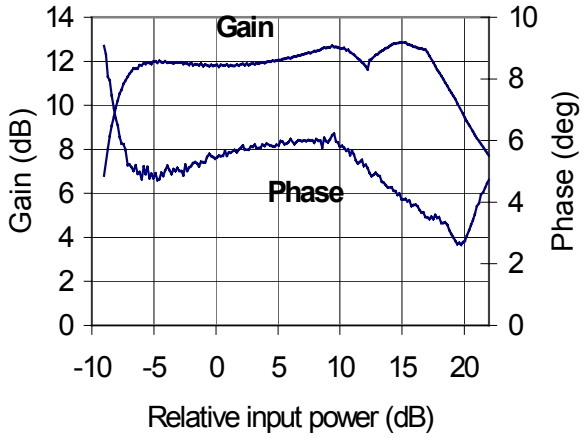

Figure 3: Relative gain and phase variation vs. input power

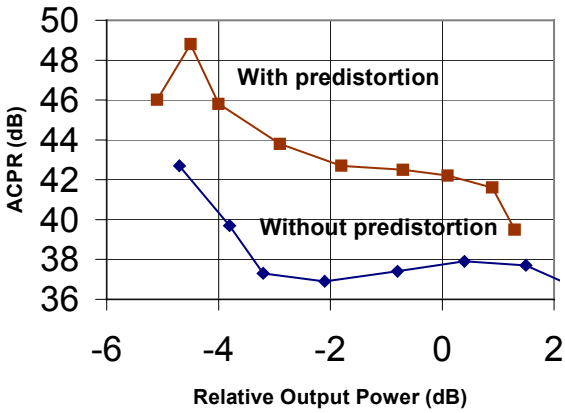

Figure 4: ACPR with or without predistortion vs. output power

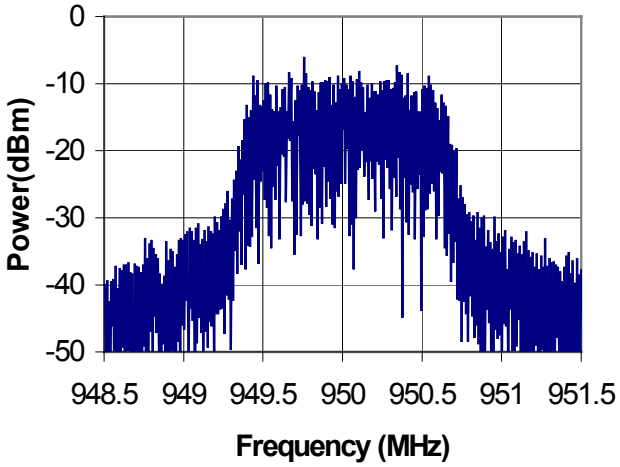

Figure 5: Spectrum without predistortion

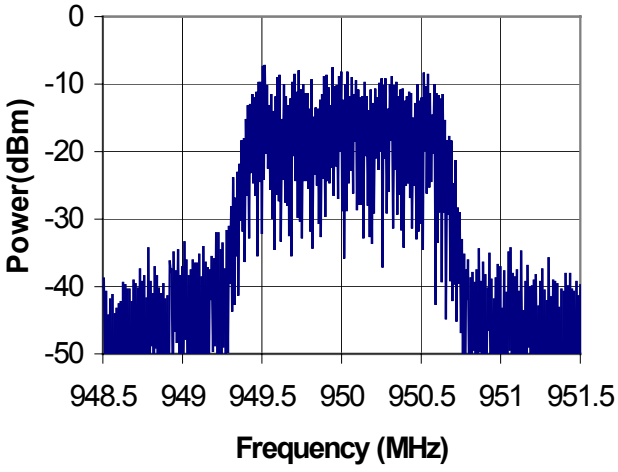

Figure 6: Spectrum with predistortion

A Highly Integrated 1 W CMOS Power Amplifier for GSM-1800

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Nokia Mobile Phones and Technical University of Denmark

Until now power amplifiers for handheld wireless applications have been produced almost exclusively in GaAs technologies, with a few exceptions in LDMOS, Si BJT and SiGe HBT. A CMOS power amplifier promises higher integration as well as lower cost. A typical power amplifier for wireless communication consists of 3 dies and 15-20 passive components plus decoupling. The CMOS power amplifier component count can be reduced to one die and 3-5 passives plus decoupling. This reduction in component count leads to a dramatic decrease of the cost.

The power amplifier presented in this work is targeted towards the GSM-1800 standard, which has a transmit frequency range of 1710 to 1785 MHz. The power amplifier is designed for a 0.35 μm CMOS process with 5 metal layers and metal-metal capacitors The power amplifier consists of two stages with integrated input and interstage impedance matching networks as well as the very first part of the output matching network. The two stages of the power amplifier operates in class AB. The schematic of the power amplifier is shown in Figure 1 and Figure 2.

The input matching network is a fully integrated highpass LC matching section. This was been chosen since it incorporates DC blocking and biasing at the same time. The inductor is a spiral inductor implemented in top metal layer, while the capacitor is made with the two lowest metal layers. The transistor of the input stage is 1 mm wide and 0.35 μm long. The input stage has an off-chip inductor acting as a RF choke (RFC). The interstage matching network consists of a LC highpass section for the same reasons as the input matching network. The implementation is made in the same way as the input matching. The output transistor is 8 mm wide and has a length of 0.35 μm, it is partioned into 6 separate finger transistors, with 30 fingers each. The output matching network is placed primarily off-chip due to efficiency considerations. In order to have better harmonic termination, a capacitor is placed on-chip, directly at the drain of the transistor, in parallel with the drain-source capacitor of the transistor. This capacitor terminates the harmonics at the drain, but at the same time it transforms the output impedance even lower. The RFC for the output stage is incorporated in the output matching network. The output matching network consists of a bandpass T section, due to the high transformation factor.

The CMOS power amplifier IC has been mounted directly on the PCB, and wire bonded directly on a goldplated PCB microstrips. The passive components used on the PCB are 0402 and 0603 SMD components. The SMA connectors have been mounted horizontally on the edge of the PCB, in order to reduce the effects of the transition from SMA connector to PCB microstrip.

The measurements were made in pulsed mode according to the GSM1800 specifications. The highest power added efficiency was 40% at 1730 MHz, with an output power of 30.3 dBm. The output power and efficiency biased for maximum power added efficiency vs. frequency is shown in Figure 4. The highest output power obtained was 31.5 dBm at 1670 MHz, with the input power increased to 15 dBm. The output power and efficiency with biases set for maximum output power vs. frequency is shown in Figure 3. The power amplifier operates on a supply voltage from 1 V to 4 V. The output power and efficiency vs. supply voltage is shown in Figure 5 The maximum output power is 32.2 dBm at 4 V.

One of the most important aspects of the reliable design of a power amplifier is accurate simulations, and a lot of emphasis was put on accurate simulations. The simulations were made in the APLAC simulator, primarily with small-signal and harmonic balance simulations, but transient simulations have also been used. The simulated and measured data was compared, a few minor modeling problems were found and corrected. The simulations showed very good agreement between the simulated and measured results, the output power were predicted within a few tenths of a dB. The comparison between simulated and measured results are shown in Figure 6.

A redesign with minor adjustments of the input and interstage matching networks will move maximum output power and efficiency to the GSM-1800 band.The die area including pads is 1.9 sq. mm. The power amplifier consists of one die, two RFCs and three matching component plus decoupling capacitors, compared to 3 dies and 15-20 passives plus decoupling capacitors for a typical GaAs power amplifier. This power amplifier gives the highest output power for a CMOS amplifier in the 1.8 GHz range. The efficiency is better than other CMOS amplifiers using linear modes[1] and comparable to or better than the switched mode approaches typically used in CMOS [1][3].

[1] Brian Ballweber, Ravi Gupta and David J. Allstot, “Fully-Integrated CMOS RF Power Amplifiers”, 1999 IEEE International Solid-State Circuits Conference

[2] David Su and William McFarland, “A 2.5-V, 1-V Monolithic CMOS RF Power Amplifier”, IEEE 1997 Custom Integrated Circuit Conference, 1997.

[3] King-Chun Tsai and P. R. Gray, “A 1.9 GHz 1-W CMOS class-E power amplifier for wireless communications”, IEEE Journal of Solid-State Circuits, July 1999, pp. 962-970.

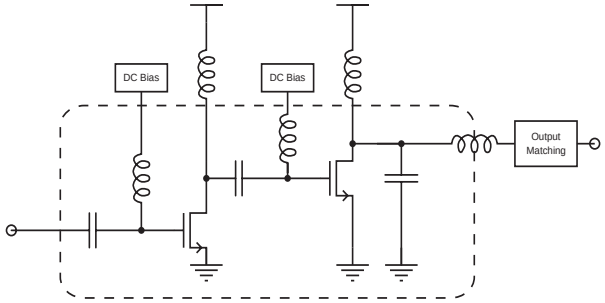

Figure 1 Schematic of the power amplifier.

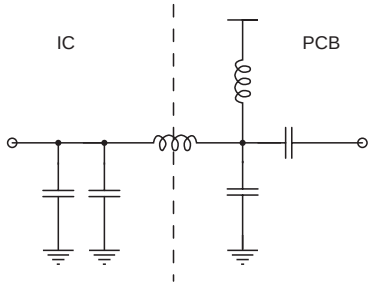

Figure 2 Schematic of the output matching network.

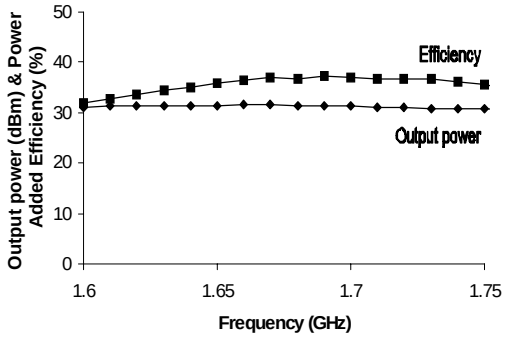

Figure 3 Measured output power and efficiency, biased for maximum output power.

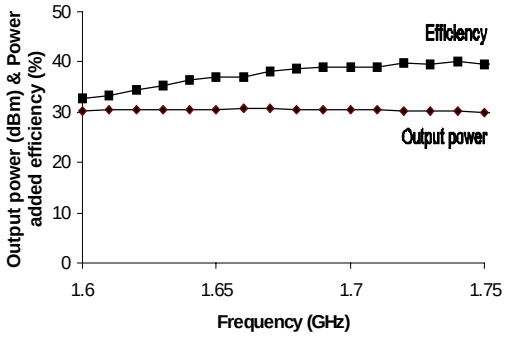

Figure 4 Measured output power and efficiency, biased for maximum power added efficiency.

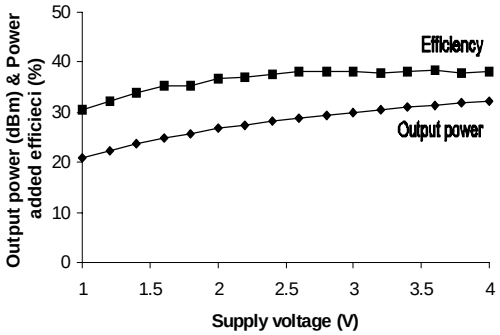

Figure 5 Measured output power and efficiency vs. supply voltage.

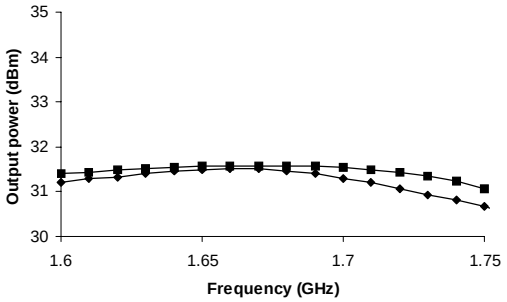

Figure 6 Comparison of simulated and measured data.

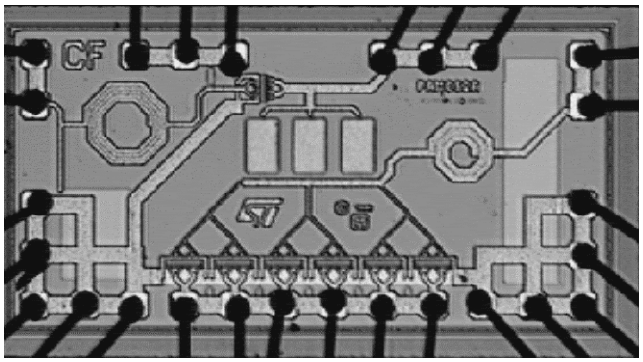

Figure 7 Photograph of the power amplifier IC

Process	0.35 µm CMOS
Supply voltage	3.5 V
Input power	5 dBm
Output power	31.5 dBm
Frequency	1710-1785 MHz
Drain efficiency	45%
Total efficiency	40%
Die area	1.9 sq. mm

Table 1. Characteristics of the power amplifier

A Highly Integrated 1W CMOS Power Amplifier for GSM-1800 with 45% PAE

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This paper presents a power amplifier designed in a 0.35 μm CMOS process. A CMOS power amplifier promises the possibility of lower cost and a higher degree of transmitter integration. The input and interstage matching networks have been fully integrated, thereby reducing the number of external components to three plus decoupling capacitors. The key features of the power amplifier are class AB operation with 31.2 dBm output power at 1730 MHz, and a maximum power added efficiency of 45%. The nominal supply voltage is 3.5 V, but the power amplifier operates down to 1.0 V. The efficiency and output power is better than reported for other CMOS amplifiers whether they use linear modes of operation or the switched mode approaches typically used in CMOS.

1. INTRODUCTION

Until now power amplifiers for wireless applications have been produced almost exclusively in GaAs technologies, with a few exceptions in LDMOS, Si BJT and SiGe HBT. The submicron CMOS processes are now usable for power amplifier design, and are without doubt the cheapest processes available. Due to the high yield in CMOS fabrication, higher integration is possible. A CMOS power amplifier therefore promises both higher integration and lower cost. A typical power amplifier module for wireless communication consists of 3 dice and 15-20 passive components plus decoupling. The CMOS power amplifier component count can be reduced to one die and 3-5 passives plus decoupling. This reduction in component count leads to a significant reduction in power amplifier cost.

Until recently, linearity of power amplifiers have not been a problem in most wireless standards. This was due to the fact that most systems, such as GSM, were constant envelope modulated, meaning that no information was stored in the amplitude. But non-constant envelope systems, such as IS-95 and WCDMA, have introduced the need for linear power amplifiers.

The problem with nonlinear power amplifiers and amplitude modulated systems is caused by spectral regrowth, due to the AM-PM conversion in the power amplifier. This means that the modulated signal will leak into the neighboring channels. The leakage is characterized by the adjacent channel power ratio (ACPR), relating the power in the channel to the power leaked into the neighboring channel.

The requirement of IS-95 is an ACPR of 26 dB. This is, however, only the start, in the 3G WCDMA wireless standards the requirement is 42 dB. Because of this, more effort will have to be placed in the design of linear power amplifiers. The linearity can be achieved by designing class A amplifiers with low efficiency or by applying linearization techniques to relatively linear power amplifiers.

The power amplifier presented in this work is targeted towards the GSM-1800 standard, which has a transmit frequency for the handset of 1710 to 1785 MHz. The goal has been to design a power amplifier with a 1 W output power with a linearity sufficient to handle the transition to 3G mobile standards, including the upcoming EDGE standard. The linearity will be improved using linearization techniques in either software or hardware. However, it is

important that the starting point is reasonable, this is the case for the designed class AB power amplifier.

2. THE DESIGNED CIRCUIT

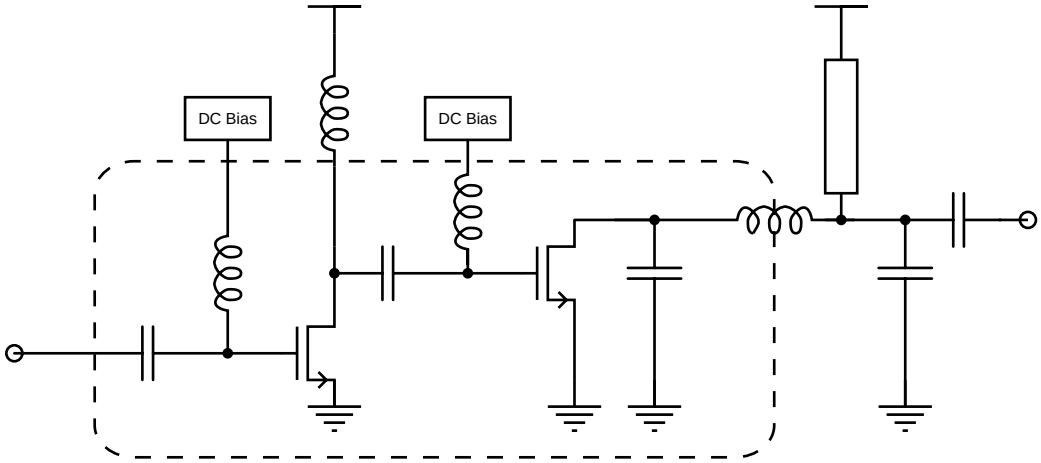

Figure 1 Schematic of the power amplifier.

The power amplifier is designed for a 0.35 μm bulk CMOS process with a substrate resistivity of 10-20 Ω-cm. The process has 5 metal layers and thin-oxide metal-metal capacitors. The special metal-metal capacitors has a high density and therefore the die size (cost) of the complete power amplifier can be reduced.

The power amplifier consists of two stages with integrated input and interstage impedance matching networks as well as the very first part of the output matching network. The schematic of the power amplifier is shown in Figure 1.The input matching network transforms the conjugate gate impedance to 50 Ω and cancels the effect of the bondwires. It is made with a fully integrated highpass LC matching section. This has been chosen because it incorporates DC blocking and biasing at the same time. The inductor is a spiral inductor implemented in the top metal layer, while the capacitor is made with the two lowest metal layers.

The input stage operates in class AB, delivering up to 15 dB gain at maximum output power. The transistor of the input stage is 1 mm wide and 0.35 μm long. The input stage has an off-chip inductor acting as a RF choke (RFC).

The interstage matching network consists of a LC highpass section for the same reasons as the input matching network. The implementation is made in the same way as the input matching, but the interstage matching transforms the gate impedance of the output transistor to the desired output load of the input stage.The output stage operates in class AB close to class B. There are a number of reasons to choose this mode of operation:

1. Class AB close to class B is relatively linear. This is not the case for class C and E amplifiers. The linearity is, however, not as good as class A.
2. The efficiency is relatively good, the theoretical maximum is 78.5%, compared with 50% for the class A amplifiers and Class C and E amplifiers have theoretical efficiencies of up to 100%.
3. The maximum drain voltage is twice the supply voltage, this is important due to the possible breakdown of the gate-oxide. Class C and E amplifiers easily exceed three times the supply voltage.
4. The power utilization factor (PUF), which is a measure of the gain compared to the output power, is reasonable compared with class A, and better than class C and E.

5. The required output load impedance is not too low to implement efficiently, which is often the case for class C.

The output transistor is 8 mm wide and has a length of 0.35 μm as the input stage. The transistor is partitioned into 6 separate finger transistors, with 70 fingers each. The gain of the output stage is approximately 12 dB.

The output matching network is placed primarily off-chip due to efficiency considerations. In order to have better harmonic termination, a capacitor is placed on-chip, directly at the drain of the transistor, in parallel with the drain-source capacitor of the transistor. This capacitor terminates the harmonics at the drain, but at the same time it transforms the output impedance even lower, leaving a more difficult matching problem. The RFC for the output stage is a relatively short microstrip which can be implemented without increasing the PCB size. The output matching network consists of a bandpass T section, due to the high transformation factor from 4 Ω to 50 Ω. The choice of the T section gives a larger bandwidth than a single L section. In the design of the network, the parasitics of the RFC microstrip has to be included.

In the design phase the two amplifier stages were initially treated separately and optimized for 50 Ω input and output matching using load-pull simulations. After each stage had been optimized an interstage matching network was designed using the impedances found for each stage.

3. SIMULATIONS

In order to make precise simulations the PCB was characterized using simple short, open and through structures. Using this approach, the transients in the SMA connector to PCB interface could be modeled accurately. The simulations of these test structures were very precise up to 4 GHz. After the SMA connectors and PCB were characterized, the output matching network was simulated and measured.

The PCB has been modeled with microstrip lines and the SMD components have been modeled according to vendor specifications. The bondwires have been modeled as inductors and the mutual coupling between the bondwires were included as well.

The measurements of the output matching network, were performed by mounting a short piece of semi-rigid cable in place of the IC. The shield of the cable was soldered to the ground plane, where the IC was supposed to be placed. The conductor of the cable was attached at the microstrip on the PCB where the bondwires from the output of the IC would go.

The IC simulations were based on parasitic extraction from the transistor and passive layout. The transistors were modeled by the MOS9 model. The spiral inductors and the metal-metal capacitors were simulated using lumped models delivered by the foundry.

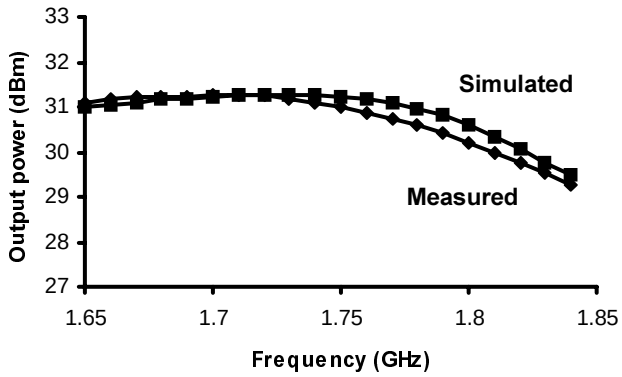

Figure 2 Comparison of simulated and measured data.

The simulations were made in the APLAC simulator, primarily with small-signal and harmonic balance simulations. For verification purposes transient simulations have been performed in the Eldo simulator. The harmonic balance simulations proved to be faster than the transient simulations, since only the steady-state solution is calculated, the precision of the simulations proved to be the same.

The simulations for the complete power amplifier including the PCB showed very good agreement between the simulated and measured results. The measured output power was predicted within a few tenths of a dB. The comparison between simulated and measured output power is shown in Figure 2.

4. MEASUREMENTS

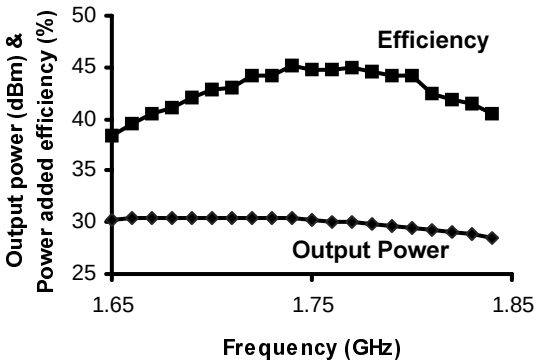

Figure 3 Output power and efficiency vs. frequency, biased for maximum efficiency

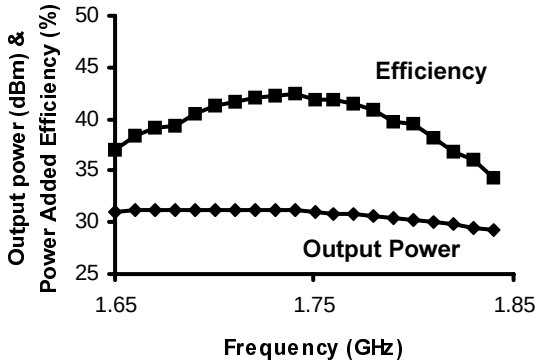

Figure 4 Output power and efficiency vs. frequency, biased for maximum output power

The CMOS power amplifier IC was been mounted directly on the PCB, and wire bonded directly onto the PCB microstrips. To enable the wire bonding, the PCB was gold plated, the dielectric used in this work was standard FR4, with a relative dielectric constant of approximately 4.3 at 1.75 GHz.

The PCB can be produced either with a PCB milling machine or at a normal PCB production facility. The first approach offers some advantages during the prototyping phase of the design. A new PCB can be built within hours, allowing for larger exploration of the design space, particularly the topology of the output matching network.

The passive components used on the PCB were 0402 and 0603 SMD components. The SMA connectors were mounted horizontally on the edge of the PCB, in order to reduce the effects of the transition from SMA connector to PCB microstrip.

To get a realistic picture of the performance, the measurements were made in pulsed mode according to the GSM1800 specifications, this means a duty cycle of 12.5%.

The highest power added efficiency was 45% at 1730 MHz, with an output power of 30.4 dBm. The output power and efficiency measurements with the power amplifier biased for maximum power added efficiency vs. frequency are shown in Figure 3

The highest output power obtained was 31.3 dBm at 1720 MHz. The output power and efficiency measurements with biases set for maximum output power vs. frequency are shown in Figure 4.

The power amplifier operates on a supply voltage from 1 V to 4 V. The output power and efficiency vs. supply voltage is shown in Figure 5 The maximum output power is 32.2 dBm at 4 V.

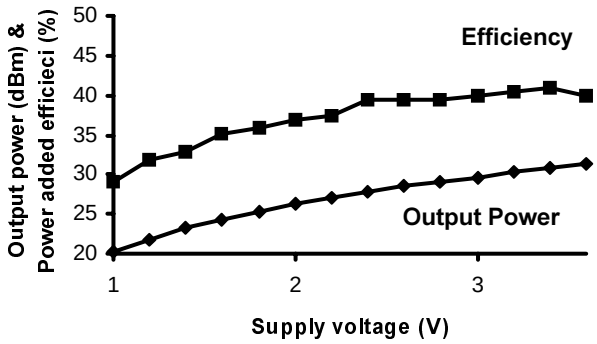

Figure 5 Measured output power and efficiency vs. supply voltage at 1730 MHz.

Due to a mismatch in the input impedance matching network, the gain of the power amplifier is lower than predicted at design time. The mismatch was caused by an error in the estimation of the parasitics of input pins.

Since the power amplifier is operating in class AB, it is inherently more linear, than e.g. the class C, D and E amplifiers demonstrated in CMOS so far [1][3][5][6]. This means that the power amplifier is suitable for digital predistortion. The adjacent channel power of the power amplifier was made without any optimizations towards lower ACPR. The measurements showed that the ACPR requirements of EDGE was met up to 2 dB from maximum required output power. At the maximum required output power the ACPR was -32 dBc, whereas the requirement of EDGE is -40 dBc. It has been shown, that an improvement of the adjacent channel power ratio (ACPR) of 8-10 dB, is possible with simple low-power digital predistortion [7][8]. This means that the power amplifier can be used for EDGE if a simple digital predistortion system is incorporated into the DSP.

A comparison of all the published CMOS power amplifier results is shown in Table 1. As can be seen from the table no other CMOS power amplifier has been published with a output power or efficiency as high as the work presented here.

	Frequency (MHz)	**P_{out} (dBm)**	**PAE (%)**	**Class**
T. Melly et. al. [1]	430	4.0	15	C
S.-J. Yoo et. al. [2]	433	13.0	30	AB
D. Su et. al. [3]	830	30.0	42	D
B. Ballweber et. al. [4]	900	19.3	23	AB
C. Yoo et. al. [5]	900	29.5	41	E
K.-C. Tsai et. al. [6]	1980	30.0	41	E
Asbeck et. al. [9]	1950	29.2	27	B
This work	**1730**	**30.4**	**45**	**AB**

Table 1. Comparison of CMOS Power Amplifiers

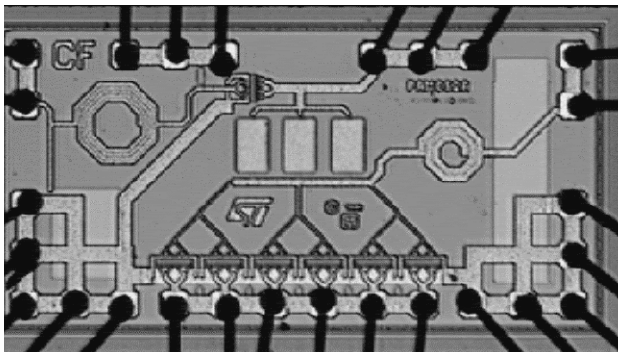

Figure 6 Die photograph

Process	0.35 µm CMOS
Supply Voltage	3.5 V
Output Power	31.2 dBm
Frequency	1710-1785 MHz
Max. PAE	45%
Die area	1.9 sq. mm

Table 2. PA summary

5. CONCLUSION

A CMOS power amplifier has been presented with a power added efficiency of 45% with an output power of 30.4 dBm at 1730 MHz. When biased for maximum output power 31.2 dBm is delivered while maintaining an efficiency of 42%. The die area including pads is 1.9 sq. mm. By accurately modeling bondwires, microstrips and SMD components the accuracy of the simulations was improved, and is now within a few tenths of a dB, compared to measured results.

The power amplifier consists of one die, one RFC, one microstrip and two matching components plus decoupling capacitors, compared to 3 dice and 15-20 passives plus decoupling capacitors for a typical GaAs power amplifier.

The power amplifier operates in class AB, which gives good output power, efficiency and linearity. Until now no CMOS power amplifiers with this output power or efficiency have been published. The fact that this power amplifier is relatively linear, means that it is useful in wireless applications, especially in systems which utilize amplitude modulation. With a digital predistortion system the power amplifier can be used for EDGE.

6. REFERENCES

[1] T. Melly, A.-S. Porret, C. C. Enz, M. Kayal and E. Vittoz, “A 1.2V, 430 MHz, 4 dBm Power Amplifier and a 250µW Front-End, using a Standard Digital CMOS Process”, 1999 International Conference on Low Power Electronics and Design, pp. 233-237.

[2] Seoung-Jae Yoo, Hong Jo Ahn, M. M. Hella and M. Ismail, “The Design of 433 MHz Class AB CMOS Power Amplifier”, 2000 Southwest Symposium on Mixed-Signal Design, pp. 26-40.

[3] David Su and William McFarland, “A 2.5-V, 1-V Monolithic CMOS RF Power Amplifier”, IEEE 1997 Custom Integrated Circuit Conference, 1997.

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[6] King-Chun Tsai and P. R. Gray, “A 1.9 GHz 1-W CMOS class-E power amplifier for wireless communications”, IEEE Journal of Solid-State Circuits, July 1999, pp. 962-970.

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[8] M. Ranjan, K. H. Koo, G. Hanington, C. Fallesen and P. Asbeck, “Microwave Power Amplifiers with Digitally-Controlled Power Supply Voltage for High Efficiency and High Linearity”, International Microwave Symposium, Boston June, 2000.

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10.3 A 1W 0.35μm CMOS Power Amplifier for GSM-1800 with 45% PAE

Carsten Fallesen, Per Asbeck

Nokia Denmark A/S, Copenhagen, Denmark

Until now, power amplifiers for wireless applications have been produced almost exclusively in GaAs technologies, with a few exceptions in LDMOS, Si BJT and SiGe HBT. The submicron CMOS processes are now usable for power amplifier design, and are without doubt the cheapest processes available and high integration is possible due to high yield. A typical power amplifier module for wireless communication consists of three die and 15-20 passive components plus decoupling. This CMOS power amplifier has one die and three passives plus decoupling. This reduction in component count leads to a significant reduction in power amplifier cost.

The power amplifier presented in this work is targeted at the GSM-1800 standard, which has handset transmit frequency of 1710MHz to 1785MHz. It is designed for a 0.35μm bulk CMOS process with a substrate resistivity of 10-20Ωcm. The process has five metal layers and thin-oxide metal-metal capacitors. The thin-oxide metal-metal capacitors are high density and therefore the die size (cost) of the complete power amplifier is reduced.
The power amplifier consists of two stages with integrated input and interstage matching. The schematic of the power amplifier is shown in Figure 10.3.1. The input matching network is made with a fully-integrated highpass LC matching section. This is chosen because it incorporates DC blocking and biasing at the same time. The inductor is a spiral inductor implemented in the top metal layer, while the capacitor is made by the two lowest metal layers.

The input stage operates in class AB, delivering up to 15dB gain. The transistor in the input stage is 1mm wide and 0.35μm long. The input stage has an off-chip inductor acting as an RF choke. The interstage-matching network consists of a LC highpass section for the same reasons as does the input matching network. The implementation is made in the same way as the input matching.

The output stage operates in class AB close to class B. The output transistor is 8mm wide and has a length of 0.35μm as does the input stage. The transistor is partitioned into 6 separate transistors, with 70 fingers each. The gain in the output stage is ~12dB. The output-matching network is placed primarily off-chip due to efficiency. To improve harmonic termination, a capacitor is placed on-chip, directly at the drain of the transistor. This capacitor terminates the harmonics at the drain, but at the same time it transforms the output impedance further down, leaving a more difficult matching problem. The RF choke for the output stage is a relatively short microstrip, which can be implemented without increasing the PCB size. The output-matching network consists of a bandpass T section, due to the high transformation factor from 4Ωto 50Ω. The choice of the T section gives a larger bandwidth than a single L section.

The CMOS power amplifier IC is mounted directly on the PCB and wire bonded directly on to the PCB microstrips. To enable the wire bonding, the PCB is gold plated. The dielectric used in this work is standard FR4, with a relative dielectric constant of ~ 4.3 at 1.75GHz.

The highest power added efficiency is 45% at 1730MHz, with an output power of 30.4dBm. The output power and efficiency measurements of the power amplifier biased for maximum power added efficiency vs. frequency are shown in Figure 10.3.2. The highest output power obtained was 31.3dBm at 1720MHz. The output power and efficiency measurements with biases set for maximum output power vs. frequency are shown in Figure 10.3.3. This power amplifier reaches higher power added efficiency and output power than any of the CMOS power amplifier previously published [1][2][3][4]. The power amplifier operates on supply voltages as low as 1V, the measured output power and efficiency vs. supply voltage are shown in Figure 10.3.4.

Simulations of the complete power amplifier including the PCB are in good agreement with measured results. The measured output power is predicted within a few tenths of a dB. Comparison between simulated and measured output power is shown in Figure 10.3.5. Since the power amplifier operates class AB, it is inherently more linear, than e.g. the class D and E amplifiers thus far reported in CMOS [1][3][4]. This means that the power amplifier is suitable for digital predistortion.

Adjacent channel power measurements of the power amplifier are without any optimizations for lower adjacent channel power ratio (ACPR). The measurements show the ACPR requirements of EDGE standard are met up to 2dB from maximum required output power. At maximum required output power the ACPR is –32dBc, whereas the requirement of EDGE is –40dBc. It is shown that an improvement of the adjacent channel power ratio (ACPR) of 8-10dB is possible with simple low-power digital predistortion [5]. This means that the power amplifier can be used for EDGE if a simple digital predistortion system is incorporated into the DSP.

A power amplifier for GSM-1800 demonstrated in a 0.35μm CMOS process has area including pads 1.9mm². The efficiency and output power are better than those of any other CMOS power amplifiers published and the linearity of the power amplifier is sufficient for EDGE.

References:

[1] D. Su and W. McFarland, "A 2.5-V, 1-W Monolithic CMOS RF Power Amplifier", Proceedings of the IEEE 1997 Custom Integrated Circuit Conference, pp. 189-192, 1997.
[2] Brian Ballweber et al., "Fully-Integrated CMOS RF Amplifiers", ISSCC Digest of Technical Papers, pp. 72-73, Feb. 1999.
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[4] K-C. Tsai and P. R. Gray, "A 1.9 GHz 1-W CMOS class-E power amplifier for wireless communications", IEEE Journal of Solid-State Circuits, pp. 962-970, July 1999.
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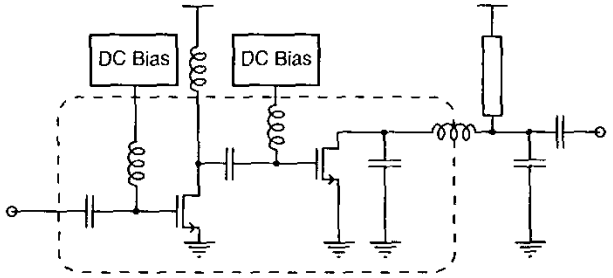

Figure 10.3.1: Schematic of the power amplifier.

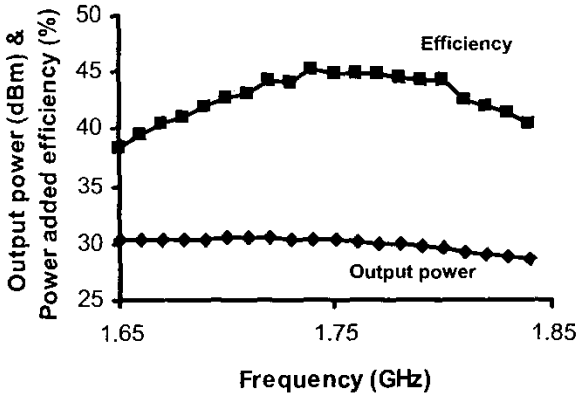

Figure 10.3.2: Measured output power and PAE at max. PAE.

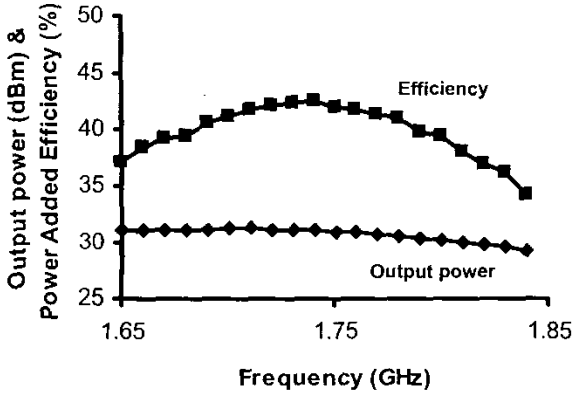

Figure 10.3.3: Measured output power and PAE at max. output.

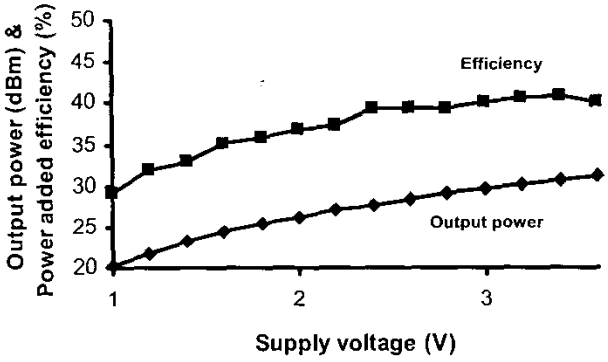

Figure 10.3.4: Measured output power and PAE vs supply voltage.

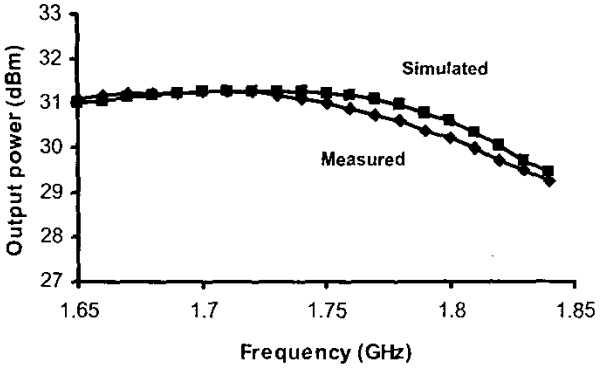

Figure 10.3.5: Comparison of measured and simulated output power.

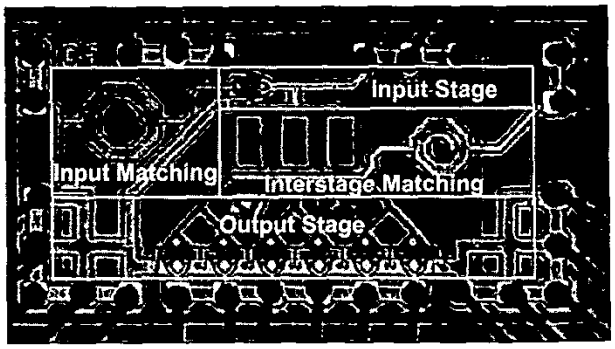

Figure 10.3.6: Power amplifier die photograph.

A 1W CMOS Power Amplifier for GSM-1800 with 55% PAE

Carsten Fallesen[1,2] and Per Asbeck[1,2]

[1]Nokia Denmark, Copenhagen, DK-1790, Denmark
[2]Technical University of Denmark, Lyngby, DK-2800, Denmark

***Abstract* -- Until recently it was the common opinion that CMOS RF power amplifiers were not feasible for mobile handsets. This paper presents a CMOS power amplifier for the GSM-1800 standard, with only two external matching components and a few decoupling capacitors. The performance of the power amplifier is better than any other CMOS power amplifier reported and comparable to commercially available power amplifier in other technologies.**

I. Introduction

This paper presents the results achieved in the design of a 1W CMOS power amplifier for GSM-1800. Due to the high yield in CMOS fabrication, higher integration is possible than e.g. in GaAs processes. A CMOS power amplifier therefore promises both higher integration and lower cost. A typical power amplifier module for wireless communication consists of 2-3 dice and 15-20 passive components. The CMOS power amplifier component count can be reduced to one die and 2-5 passives plus decoupling. This reduction in component count leads to a significant reduction in power amplifier cost.

The power amplifier presented in this work is targeted towards the GSM-1800 standard, which has a transmit frequency for the handset of 1710 to 1785 MHz. The goal has been to design a power amplifier with a 1 W output power

II. Design

The design of this power amplifier followed the design and simulation methodologies described in [1]. The design is the second iteration of a 1W CMOS power amplifier for GSM-1800, results of the first iteration have previously been presented [2]. This power amplifier shows higher integration and much better efficiency than previously presented.

The power amplifier is designed for a 0.35 µm bulk CMOS process with a substrate resistivity of 10-20 Ω-cm. The process has 5 metal layers and thin-oxide metal-metal capacitors. The thin-oxide metal-metal capacitors have a high density and therefore the die size (cost) of the complete power amplifier can be reduced.

The first choice to make was the number of stages in the power amplifier. In this case a two-stage methodology was chosen.

Then the class of operation was chosen for each of the stages. The input and output stages operates in class AB close to class B. There are a number of reasons to choose this mode of operation:

1. Class AB close to class B is relatively linear. This is not the case for class C and E amplifiers. The linearity is, however, not as good as class A.
2. The efficiency is relatively good, the theoretical maximum is 78.5%, compared with 50% for the class A amplifiers and Class C and E amplifiers have theoretical efficiencies of up to 100%.
3. The maximum drain voltage is twice the supply voltage, this is important due to the possible breakdown of the gate-oxide. Class C and E amplifiers easily exceed three times the supply voltage.
4. The power utilization factor (PUF), which is a measure of the gain compared to the output power, is reasonable compared with class A, and better than class C and E.
5. The required output load impedance is not too low to implement efficiently, which is often the case for class C.

Once the class of operation was chosen for the output stage it was possible to start the dimensioning of the output transistor. This dimensioning was an iterative process where the initial guess originated from the I-V characteristic of the power amplifier. From the I-V characteristic it was possible to find the voltage and current swings possible for a given load-line. From the voltage and current swings the maximum output power was then determined and a reasonable size of the transistor was found.

After an initial value is selected the more accurate RF behavior is found using load-pull simulations. The load-pull simulations are the simulation equivalent of the load-pull measurements.

The final schematic of the power amplifier is shown in Fig 1 where the components mentioned below can be located. The output transistor (M_2) was then chosen to be 8 mm wide and with a length of 0.35 µm. The transistor is partitioned into 6 separate finger transistors, with 70 fingers each. The input stage also operates in class AB. The transistor of the input stage (M_1) is 1 mm wide and 0.35 µm long.

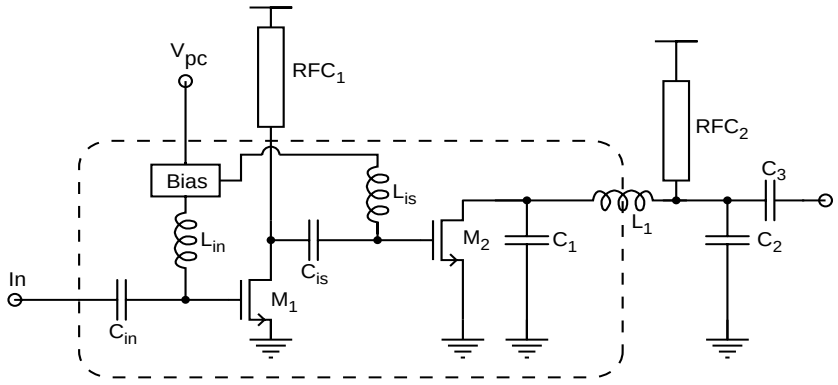

Fig 1. Simplified schematic of the power amplifier.

The output matching network is placed primarily off-chip due to efficiency considerations. In order to have better harmonic termination, a capacitor (C_1) is placed on-chip, directly at the drain of the transistor, in parallel with the drain-source capacitor of the transistor. This capacitor terminates the harmonics at the drain, but at the same time it transforms the output impedance even lower, leaving a more difficult matching problem. The RF chokes (RFC_1, RFC_2) for the output stage as well as the input stage are relatively short microstrips, which can be implemented without increasing the overall PCB size. The output matching network consists of a bandpass T section (L_1, C_2, C_3), due to the high transformation factor from 4 Ω to 50 Ω. The choice of the T section gives a larger bandwidth than a single L section. The inductor in the T section consists of a contribution from the bondwires as well as from the microstrip. In the design of the network, the parasitics of the RFC microstrip were also included.

The input and interstage matching networks were both made with a fully integrated highpass LC matching section. This was chosen because it incorporates DC blocking and biasing at the same time as the impedance matching. The on-chip inductors are spiral inductors implemented in the top metal layer, while the capacitors are made thin-oxide metal-metal capacitors in the two lowest metal layers.

III. Measurements

The CMOS power amplifier IC was been mounted directly on the PCB and wire bonded directly onto the PCB microstrips. To enable the wire bonding, the PCB was gold plated, the dielectric used in this work was standard FR4, with a relative dielectric constant of approximately 4.3 at 1.75 GHz.

The passive components used on the PCB were 0402 SMD components. The SMA connectors were mounted horizontally on the edge of the PCB, in order to reduce the effects of the transition from SMA connector to PCB microstrip. The die photo is shown in Fig 5 while the PCB is shown in Fig 4.

To get a realistic picture of the performance, the measurements were made in pulsed mode according to the GSM1800 specifications, this means a duty cycle of 12.5%.

The highest power added efficiency was 55% at 1750 MHz, with an output power of 30.4 dBm. The output power and efficiency measurements with the power amplifier biased for maximum power added efficiency vs. frequency are shown in Fig 1.

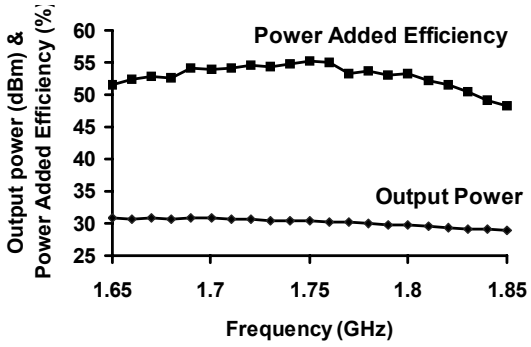

Fig 1. Output power and power added efficiency vs. frequency.

The power amplifier operates on a supply voltage from 1 V to 3.4 V. The output power and efficiency vs. supply voltage is shown in Fig 2. The output power is 20.8 dBm at 1V and 31.4 dBm at 3.4 V. The power added efficiency varies from 43% to 55% at 1V and 3.4V respectively.

A comparison of all the published CMOS power amplifier results is shown in Table I. As can be seen from the table no other CMOS power amplifier has been published with output power or power added efficiency as high as the work presented here.

The simulations for the complete power amplifier including the PCB showed very good agreement between the simulated and measured results. The measured output

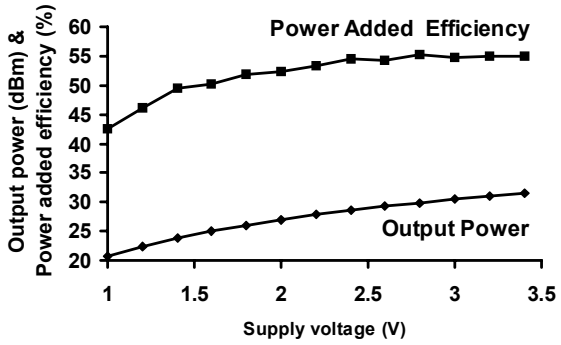

Fig 2. Measured output power and power added efficiency vs. supply voltage at 1750 MHz.

power was predicted within a few tenths of a dB. The efficiency deviated less than 1%. The comparison between simulated and measured output power is shown in Fig 3.

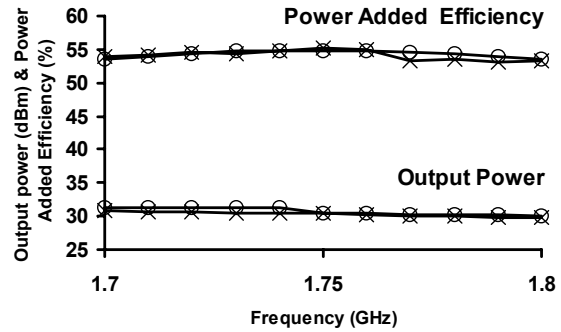

Fig 3. Comparison of simulated and measured data.

IV. Conclusion

A CMOS power amplifier has been presented with a power added efficiency of 55% with an output power of 30.4 dBm at 1750 MHz. The power amplifier is designed for GSM-1800 with a supply voltage of 3V, although it performs very well from 1V to 3.4V. The die area including pads is 1.1 sq. mm. By accurately modeling bondwires, microstrips and SMD components the accuracy of the simulations was within a few tenths of a dB, compared to measured results.

The power amplifier consists of one die, two short microstrips and two matching components plus decoupling capacitors, compared to 3 dice and 15-20 passives plus decoupling capacitors for a typical GaAs power amplifier. The power amplifier has higher power added efficiency than any other CMOS power amplifier results published so far, whether they operate linearly [3][4][5][2] or nonlinearly [6][7][8][9].

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[9] K.-C. Tsai and P. R. Gray, "A 1.9 GHz 1-W CMOS class-E power amplifier for wireless communications," *IEEE Journal of Solid-State Circuits*, July 1999.

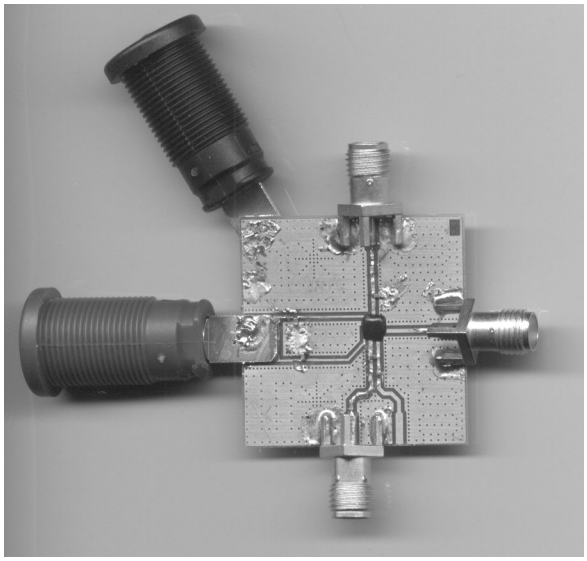

Fig 4. PCB photograph.

TABLE I

COMPARISON OF CMOS POWER AMPLIFIERS.

	Frequency (MHz)	**P_{out} (dBm)**	**PAE (%)**	**Class**
T. Melly et. al. [6]	430	4.0	15	C
S.-J. Yoo et. al. [3]	433	13.0	30	AB
D. Su et. al. [7]	830	30.0	42	D
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C. Yoo et. al. [8]	900	29.5	41	E
K.-C. Tsai et. al. [9]	1980	30.0	41	E
Asbeck et. al. [5]	1950	29.2	27	B
Fallesen et. al. [2]	1730	30.4	45	AB
This work	***1750***	***30.4***	***55***	***AB***

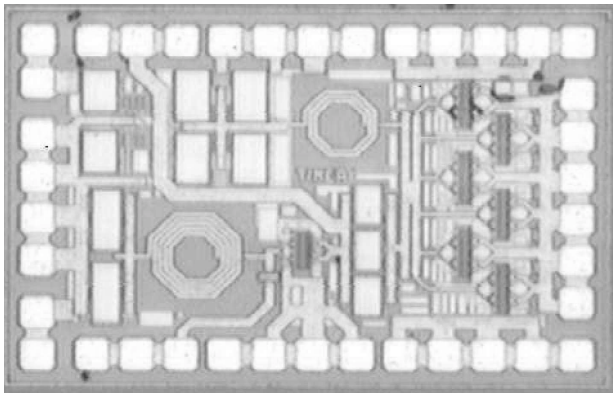

Fig 5. Die photograph.

MICROWAVE POWER AMPLIFIERS WITH DIGITALLY-CONTROLLED POWER SUPPLY VOLTAGE FOR HIGH EFFICIENCY AND HIGH LINEARITY

M. Ranjan, K.H. Koo*, G. Hanington, C. Fallesen** and P. Asbeck
University of California, San Diego
*University of Inchon, Inchon, Korea
** Nokia Mobile Phones, Copenhagen

ABSTRACT

A power amplifier architecture is presented which comprises a basic amplifier with an efficient, high modulation bandwidth DC-DC converter. The amplifier and the DC-DC converter are controlled by a digital signal processor that provides input signal pre-distortion, supply voltage optimization and equalization. Experimental results at 950MHz showed ACPR values acceptable for IS-95 CDMA handset applications. With variable power supply, the overall efficiency improved by a factor of 1.4x (when averaged over representative conditions of usage).

INTRODUCTION

Efficiency of power amplifiers can be significantly improved by employing a DC-DC converter which varies the power supply voltage in accordance with the envelope of the input signal [1-2]. This technique (known as "envelope tracking" or "dynamic supply voltage" amplifier) improves the amplifier efficiency when the output power is below its saturated value, which can be a large fraction of the time in cellular phone applications.

In past work [1], we have shown that such amplifiers can be implemented using GaAs HBT-based DC-DC converters, which can be modulated at bandwidths of 1MHz, and have efficiencies of up to 80%. The power supply control voltage was derived from an analog envelope detector.

Amplifiers based on this architecture have inherent non-linearities associated with them. Non-linearities stem from two sources. One source is the fact that the amplifier gain and phase characteristics change with a change in the power supply voltage, and thus the signal dependent power supply voltage is a source of AM-AM and AM-PM distortion. The other stems from the time delay and the finite frequency response of the DC-DC converter.

In this work we demonstrate that digital control of the DC-DC converter, coupled with digital predistortion of the amplifier input signal, can improve the amplifier linearity while optimizing efficiency. Application of DSP allows flexibility in the algorithm for power supply selection, ability to equalize the delay and the frequency response of the DC-DC converter, as well as ability to predistort the RF signal to overcome the associated AM-AM conversion.

The amplifier architecture reported here is a significant step towards realization of a "smart" power amplifier, in which the amplifier parameters are dynamically varied in accordance with the signal requirements in order to maximize performance.

AMPLIFIER STRUCTURE

A GaAs MESFET amplifier was used in conjunction with a DC-DC converter implemented with a GaAs HBT, as shown schematically in Fig.1a and b. Fig 1a shows the previously reported system based on an envelope detector to control the power supply voltage; Fig 1b illustrates the modified DSP-based system reported in this paper.

GaAs HBT based DC-DC converters were implemented as hybrid circuits or as partially integrated circuits. The converter efficiency was approximately 80%.

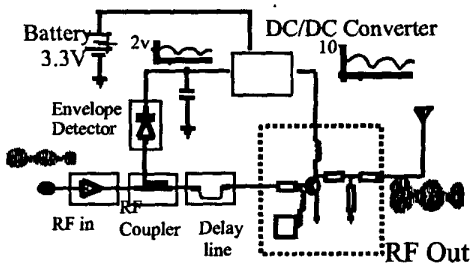

Figure 1a: Amplifier architecture with dynamic supply voltage under analog control

Fig. 2 shows the relationship between power supply voltage and instantaneous output power that was implemented, and for comparison the peak-to-peak voltage swing at the given output power.

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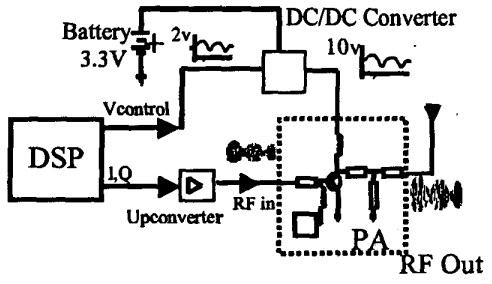

Figure 1b: Amplifier architecture with dynamic supply voltage under digital control

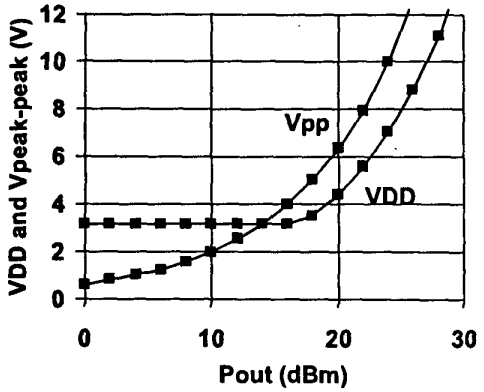

Fig.2: Algorithm of VDD vs output power. Also shown is peak-to-peak drain voltage

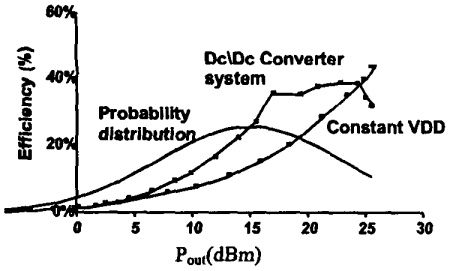

Fig.3: Measured efficiency of amplifier with constant VDD and with dc/dc converter , at different output power levels. Also shown is a representative distribution of output power for wireless application.

The choice of supply voltage kept the amplifier in Class AB operation over a wide range of output powers. The overall system efficiency depends on the efficiency of the amplifier at different power levels and the efficiency of the DC-DC converter. The efficiency of the system is shown as a function of output power in Fig.3. This demonstrates that while at maximum output power the inclusion of the DC-DC converter is detrimental to efficiency, at lower output powers it is highly advantageous. A suitable average efficiency can be computed based on power usage probabilities. A representative probability distribution of output power in cellular phone applications is shown in Fig. 3. The overall efficiency increases by a factor of typically x1.4

The linearity of the dynamic supply voltage amplifier is typically worse than the amplifier with fixed supply voltage because of the variation of gain with supply voltage. The power amplifier gain as a function of output power at various power supply voltages is shown in Fig.4. No particular design optimization of the MESFET-based amplifier was done to minimize the gain variations. From these data, substantial changes in gain as a function of output power could be inferred, leading to undesirable AM-AM conversion. We have shown that fixed predistortion can be used to overcome this nonlinearity to a considerable extent [4]. Part of the distortion, however, cannot be compensated within the framework of a memoryless nonlinear system since there is an inherent delay and a frequency-dependent transfer function between the measured signal envelope and the DC-DC converter output. The frequency response of the DC-DC converter displays a roll-off at frequencies above 700kHz. Fig. 5 shows the frequency response of the DC-DC converter. The technique reported here allows for compensation of all these sources of nonlinearity (on an open loop basis).

ALGORITHM

The DSP computes an appropriate control voltage for the DC-DC converter according to the signal envelope, taking into account the DC and AC response of the converter. It also computes a predistorted input signal for both the I and the Q channel to be fed into the amplifier, using the amplifiers AM-AM and AM-PM characteristics for this supply voltage.

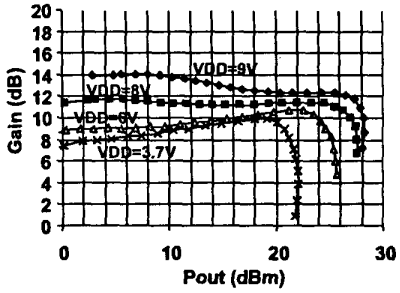

Fig. 4: Measured variation of PA gain with V_{dd}.

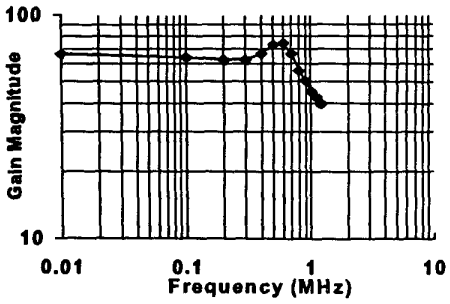

Fig. 5: Frequency response of the DC-DC Converter

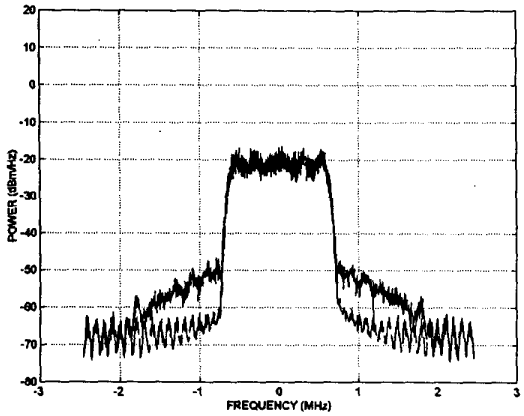

Fig. 6: Simulated amplifier output, with and without predistortion

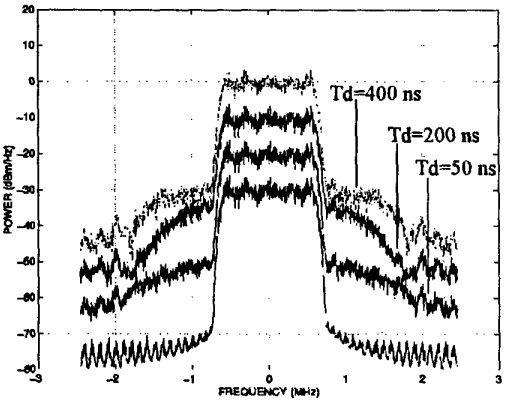

Fig. 7: Amplifier response to the predistorted input with different time delays in the DC-DC converter

The predistorted I and Q are given by:

$$I_d = (1/G_d)(I\cos\phi_d + Q\sin\phi_d) \quad (1)$$

$$Q_d = (1/G_d)(-I\sin\phi_d + Q\cos\phi_d) \quad (2)$$

where G_d and ϕ_d describe the gain and phase deviations of the amplifier as a function of input power induced by the power supply variation. The DSP computations are carried out at baseband. The I and Q signals must then be upconverted and amplified to provide the inputs to the power amplifier. In a cellular phone realization the computations can be performed in the same DSP that generates the conventional signal. In our experiments, the signals were precomputed using MATLAB in a conventional PC, and then stored in the memory of arbitrary waveform generators (high speed digital-to-analog converters). They were subsequently read out and upconverted to feed into the power amplifier. Fig. 6 shows the simulated amplifier response to the input signal with and without predistortion, indicating that the AM-AM and AM-PM of the amplifiers are significant and can be overcome by predistortion (at least under optimal conditions). Fig. 7 shows the simulated amplifier response to the predistorted input signal with different time delays introduced into the DC-DC converter. The results indicate that the ACPR is quite sensitive to the timing relationships between the supply voltage and input signal.

EXPERIMENTAL RESULTS

With the use of the DSP, the output frequency spectrum for an IS-95 CDMA input signal was considerably improved. A representative output spectrum for an output power of 28dBm is shown in Fig. 8 (together with the spectrum obtained without predistortion for comparison). An improvement of 8 dB in ACPR was observed. The value of ACPR with predistortion is –44 dBc (which exceeds the IS-95 minimum specification of -42dBc) at the largest output power (and is better at lower output power). The linearization by DSP allows increasing the output power by about 4 dBm (and thus improving efficiency) while staying within the specifications of the IS-95 signals.

CONCLUSIONS

An amplifier architecture is demonstrated which can provide improved efficiency and linearity for CDMA signals. The architecture employs a high speed DC-DC converter, which can be integrated with the power amplifier [5] and DSP control over amplifier input signal as well as power supply voltage. The system can flexibly implement a variety of algorithms for system optimization. Application of DSP to amplifier control is becoming increasingly cost-effective [6]. However, this approach requires integrated design of the overall transmitter since

the DSP function and the power amplifier must be closely coupled.

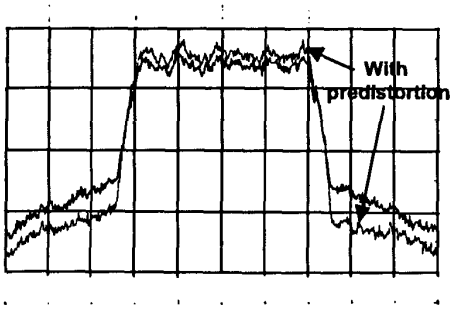

Fig.8: Measured output power spectra for an IS-95 CDMA signal with and without predistortion and equalization (30 kHz resolution bandwidth, 3MHz span). The corresponding ACPR values are –44dBc and –36dBc.

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A RF POWER AMPLIFIER IN A DIGITAL CMOS PROCESS

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ABSTRACT

A two stage class B power amplifier for 1.9 GHz is presented. The amplifier is fabricated in a standard digital EPI-CMOS process with low resistivity substrate. The output power is 29dBm in a 50 Ohm load. A design method, based on sweeping the loss and the resonant frequency of a LC tank to determine large signal parameters of the output transistor, is presented. Based on this method, proper values for on-chip interstage matching and off-chip output matching can be derived. Measurement of a fabricated chip is compared with the simulated circuit.

1 INTRODUCTION

The continuing reduction in production cost and the fast improvement of technology within personal communication systems makes it possible to extend the market and reach most people. The CMOS technology has played an important role in providing high functionality and complexity at low costs. For cheap wireless terminals it is attractive to integrate the RF front-end with the back-end signal processing to reduce assembly cost. Also if expensive RF technologies such as GaAs could be avoided in the design, costs could be reduced. For A RF Power Amplifier the problem is even more severe due to the limited voltage handling capability (breakdown). The reason that the integration has not been achieved is due to the lack of RF CMOS performance. The linearity and power efficiency seem to be lower given a certain power budget.

If the linearity problem could be solved, the front-end could be integrated, maybe at the price of lower power efficiency.

This is the motivation for the present work. We want to design a power amplifier that supports linear modulations schemes such as QPSK either by having sufficient linearity, or by using linearization techniques, such as Cartesian Modulation feed back, to enhance the linearity. The foundation for being able to utilize linearization techniques is that the PA itself is fairly linear to ensure stability.

In this paper we describe a class B power amplifier (PA) implemented in a mainstream digital CMOS technology. Unlike class E amplifiers, which have got a lot of attention lately [4] due to a good power efficiency, class B amplifiers are inherently more linear.

This text is divided into the following sections: section 2 discusses limitations of CMOS power amplifiers. Section 3 describes the power transistor and the matching network. Section 4 describes the gain stage, the interstage matching network and passives. Section 5 deals with the layout. Section 6 presents measurements of the fabricated chip and section 7 draws the final conclusions.

2 LIMITATIONS OF A CMOS PROCESS

The power amplifier output stage is limited by the following factors. The first important factor is the limitation in a CMOS process of a low gate oxide break down voltage (~5V for 5nm gate oxide). This voltage limits the maximum gate-drain voltage and thereby the maximum supply voltage. Depending on the class of operation (B,C,E) of the output stage, the relation between the maximum drain voltage and the supply voltage varies. For class B operation the ratio is 2, whereas for class E the ratio is 2-5 [1]. Therefore, a class E amplifier requires a lower supply voltage for the same breakdown voltage.

The second limitation is the low output impedance of the PA. To achieve a high output power, a low effective resistive load ($R_{effective}$ in figure 1) must be chosen. The result is a high sensitivity to parasitic resistance in the matching circuits and a complicated matching circuit due to a higher transformation ratio.

The third limitation of the output stage is the maximum PA output current needed to achieve the required power in the load. The current may be so high that electromigration and parasitics in the circuit cause performance degradation.

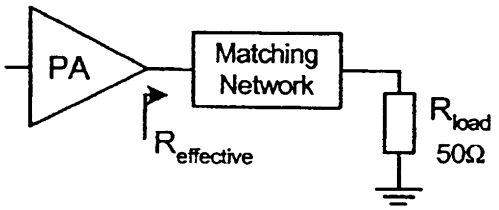

Figure 1. Power amplifier and load

3 DESIGNING THE OUTPUT STAGE

Due to linearity and the ability to operate at low supply voltages a class B output stage is chosen. A method to find the optimum load and the large-signal effective drain-source capacitance is described.

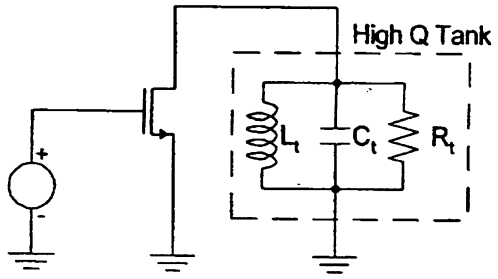

Figure 2. Determination of effective transistor load using a high Q tank.

The size of the output transistor is determined using the circuit shown in figure 2. A high Q tank is used as a load which eliminates the effect of the drain-source capacitance. Furthermore the tank filters the harmonic of the carrier frequency so a load for the carrier frequency is found. A simulator which takes large signal nonlinearity into account is used. Harmonic balance or transient simulation are suitable. A bias voltage corresponding to the threshold voltage of the transistor is required for class B operation. The RF voltage swing should be chosen

large enough to allow the transistor to get close to the triode region. This can be determined from a standard Ids-Vgs plot.

Sweeping the resistor, R_t, representing the LC tank-loss, the optimum large signal working condition can be found. Such a sweep is depicted in figure 3. By varying the transistor width and sweeping the tank loss, the load for optimal output power or power efficiency can be found.

For an output power of 1 Watt and a width of 10000µm a drain efficiency of 68% was achieved. The efficiency should of course be taken with caution as losses in the matching network are neglected. The amplitude of the gate signal was 1 Volt which can easily be provided by a driver stage, as the supply voltage is 3 Volt.

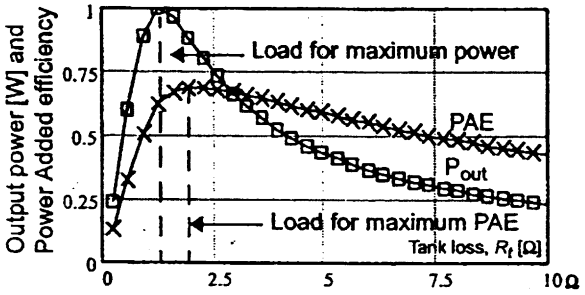

Figure 3. Simulated normalized output power (square) and PAE (cross) versus tank loss

If the Q value of the tank is lowered (5-10) so the influence of the drain-source capacitance can not be neglected, a displacement in frequency of the optimum load is observed. Then the frequency displacement can be used to calculate the large signal drain-source capacitance the following way:

$$C_{ds,\,effective} \cong 2 \cdot \frac{Q}{R \cdot \omega_c} \cdot \left(\frac{\omega_{peak}}{\omega_c} - 1 \right) \qquad \text{(EQ 1)}$$

Now a large signal model for the output transistor is available in the sense that an optimum resistive load and an effective drain-source capacitance are available. If the matching network establishes the effective resistance and cancels the calculated effective drain-source capacitance, the required RF operation of the transistor is ensured. The design of a matching circuit for the 50 Ohm load is now a simple matching exercise.

4 GAIN STAGE AND INTERSTAGE MATCHING

In this design a standard digital 0.25µm EPI-CMOS process is used. This process provides sufficient gain to achieve the desired gain of 20 dB with two stages (figure 4).

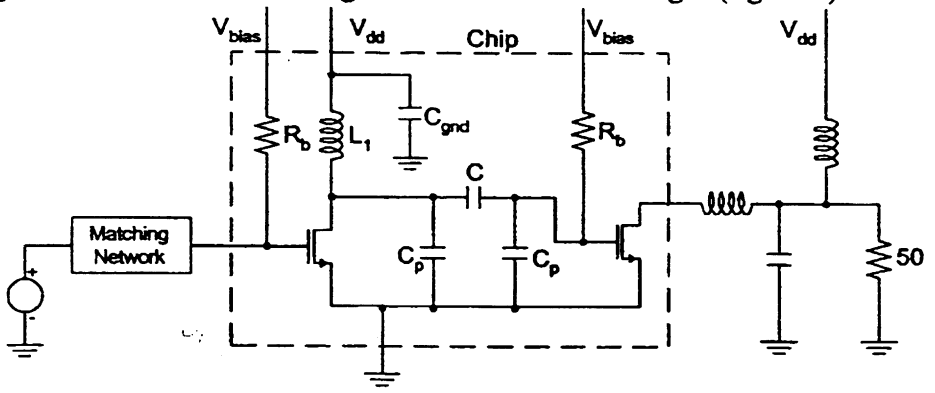

Figure 4. Fabricated PA circuit

In order to control the DC bias voltage of the output transistor independently of the drain voltage of the input transistor, a big capacitor, *C*, of 20pF is inserted. The parasitic capacitance to the substrate will be significant, because the actual capacitor requires a large area as no thin

oxide for the MIM capacitors is available. The on-chip inductor, L_1, resonates out the parasitic capacitance consisting of the gate capacitance of the output transistor and the parasitics of the on-chip DC block capacitor, C_p. A simple but realistic inductor model derived from the current sheet model [6] was used in the design phase, which made it possible to find the inductor within a few iterations. Below the inductor, a grounded poly shield [7] (see chip photo figure 7) was placed to prevent capacitive coupling to the substrate. Losses will still be introduced in the low resistivity substrate ($10m\Omega$-cm) due to the magnetic field, which together with the resistive wire-loss limits the Q-values to a maximum of 5 or 6. The final inductor was verified by the inductor simulator program, ASITIC, and showed agreement within 5% of the simple model.

The input transistor operates in class A and is sized to cancel the losses of the inductor and to provide a voltage swing of 1V on the gate of the output transistor (see section *"Designing the input stage"*). The bias voltage is provided though a 400 Ohm on-chip resistor to avoid loading the AC signal on the gate.

5 LAYOUT

The layout (figure 5) of the PA was in 0.25µm, 6 metal layers digital CMOS process. Two large capacitors are used. The DC block capacitor in the middle of the layout was realized as lateral flux capacitors in metal 3 and metal 4, whereas metal 5 and 6 were layed out as plates on top.

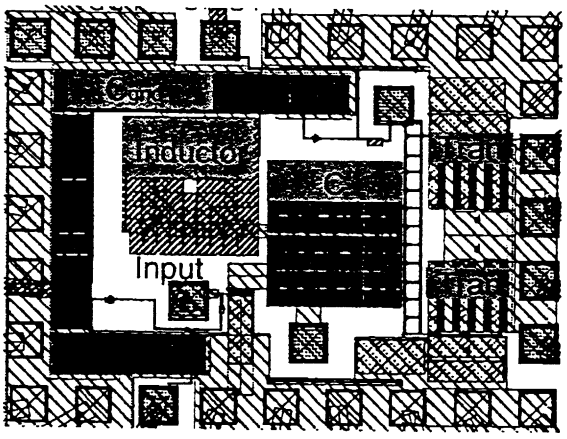

Figure 5. Layout of the PA

The reason why lateral flux capacitors were used for metal 3 and 4 is that the spacing between adjacent metal is smaller (0.4µm) than the spacing between two different metal layers (0.9µm). Utilizing metal layers 3,4,5 and 6, a capacitance density of approximately 0.19 fF/µm^2 is achieved. Metal layer 1 and 2 are not used, to limit the coupling to the substrate. The DC block capacitor is approximately 20pF. The grounding capacitor, C_{gnd}, in figure 4 is realized using all metal layers. The density of this capacitor is approximately 0.39 fF/µm^2. The total capacitance is 46 pF. The capacitor value is estimated based on the area of adjacent metal layers and the plate capacitor formula. The output transistor is folded to minimize the drain and source area. The maximum width of each folded transistor is 12µm to ensure a small gate resistance and thereby a fast transistor. Also after every 5th transistor, a column of substrate contacts is inserted to ensure a low resistance to the substrate. The ground bonding inductance should be minimized using many ground pads and bonding wires. In this design 19 ground pads were used.

The on-chip inductor was realized in metal layer 6 with a poly shield to reduce capacitive coupling to the substrate (see figure 7)

6 SIMULATIONS AND MEASUREMENT

A printed circuit board (PCB) was designed and the bare PA-chip was glued directly on the print and bonded (chip on board). Thereby the shortest possible bondwires were achieved. The maximum output power was measured as 29.2 dBm (see table 1) at the frequency of 1.95 GHz, which to our knowledge is the best performance reported for a class B power amplifier in standard digital CMOS process. In [3] and [2] an output of 13dBm and 19.3dBm respectively were achieved for a class AB PA. In [9] an output power of 31.2dBm was achieved with a CMOS process with high resistive substrate (10-20 Ω-cm) and analog options. High resistive substrate is an advantage for RF-circuits because the inductors achieve 50-100% higher Q-values and the PA-gain is higher dissipating the same amount of power. Further the process benefits from thin oxide MIM capacitors which leads to lower parasitic capacitance of the on-chip capacitors. The results achieved for the CMOS PAs [4],[5],[8] are 30dBm but these operate in class C and E which unlike class B are non-linear modes of operation. The power added efficiency of our PA was 27.4% which is approximately the same as for the two other class B CMOS amplifiers (23% in [3] and 30% in [2]).

The small signal power gain was 20.7 dB. A measured power sweep depicting the gain, PAE and output power is shown in figure 6. The used frequency is the center of the uplink frequency band of UMTS which was the design target.

The initially simulated output power was 1W and the maximum measured output power was 0.84W. The difference is due to PCB parasitics such as wire inductance and wire capacitance. Furthermore the discrete components in the matching network cause losses. We model the PCB wires with strip lines and the components in the matching network with finite Q models and achieved a result within 5% of the measured output power.

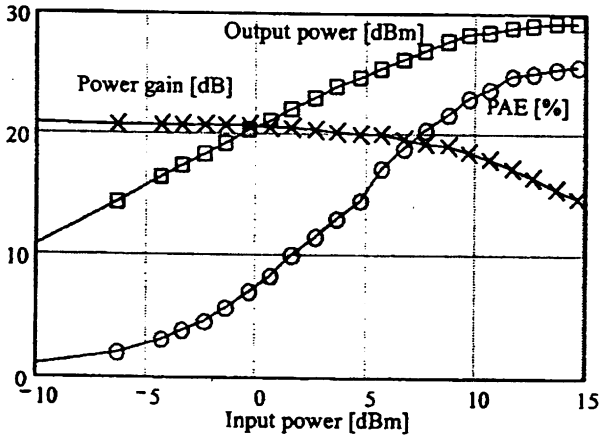

Figure 6. Measured PA characteristic

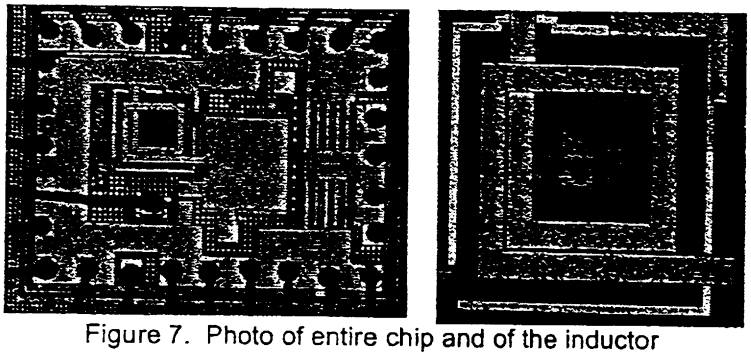

Figure 7. Photo of entire chip and of the inductor

7 CONCLUSION

A 1.9GHz class B power amplifier was designed in digital 0.25μm CMOS process. The designed and fabricated PA delivered an output power of 29.2 dBm (0.84W) which to our knowledge is the best result for a class B power amplifier in a standard digital CMOS process with low resistivity substrate. Agreement within 5% between measurement and simulation was achieved by carefully modeling wires and discrete components of the PCB. A design method based on deriving large signal parameters of the output transistor using an LC tank was presented. The design method and the models of the passives, on-chip inductor and lateral flux capacitors were described.

Table 1. Measured PA characteristic

Property	Value
Process	0.25μ CMOS
Supply voltage [V]	3
Frequency [GHz]	1.95
Max Power [dBm]	29.2
PAE [%]	27.4
small signal gain [dB]	20.7
large signal gain [dB]	14.2

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A Polar Linearisation System for RF Power Amplifiers

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Abstract: An new transmitter architecture for polar linearization of RF power amplifiers is presented. The architecture is adapted to digital transmitters which makes it possible to move some of the analog signal processing to the digital domain. An improvement of the varying loop-gain problem in feed back linearisation systems, that is easily incorporated in the new architecture is presented. This improvement increases the stability margin and reduces the variations of the bandwidth which leads to higher linearity of the system. Simulations documenting the improvements and showing important design constraints are presented.

1. Introduction

The enormous growth in mobile phones and wireless terminals together with the limited allocation of frequency bands leads to a wish for better utilization of the bandwidth available.

The improvement needed to allow higher throughputs requires a modulation scheme that modulates the amplitude and the phase of the carrier considerably. At the transmitter side this leads to high linearity requirements to prevent a degradation of the signal quality and to prevent disturbance of neighbour channels (spectral leakage). To accommodate linearity and high power efficiency, which are normally trade offs, linearisation systems come into use. Based on predistortion, feed-forward and feed back techniques, the system tries to compensate for the non-linearity of the RF power amplifier [1].

In the following we present a new architecture for a polar linearization which uses the existing digital signal processor (DSP) in the transmitter to eliminate some analog signal processing blocks. Furthermore an enhancement to the architecture which is easily implemented in the new architecture is presented. The enhancement alleviates the loop-gain problems and the stability problems The architectures are suited for monolithic integration [2].

System simulations based on the GSM/ EDGE system [5] and a measured power amplifier (PA) are carried out to evaluate the achievable performance.

2. Polar linearisation in a digital transmitter.

A polar modulation feed back linearisation system ([2],[3]) is shown in figure 1. The system is not optimal for modern digital transceivers because the essential signals (amplitude and phase) are derived by analog circuits.

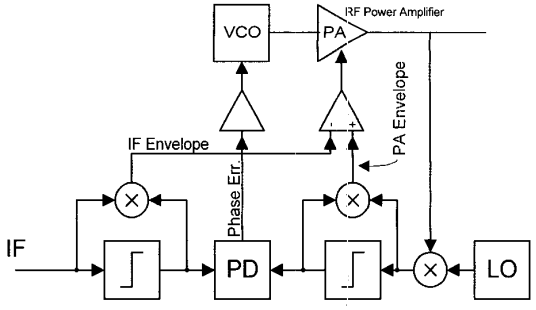

Fig. 1. Traditional polar modulation feedback.

We suggest an architecture (figure 2) that generates the essential signals digitally and allow us to eliminate a limiting amplifier and a mixer. The signals used for linearisation in figure 2 propagates through less analog circuits and are therefore more linear and less noisy. Furthermore, this kind of signal processing is

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handled more power efficient and precise in the DSP.

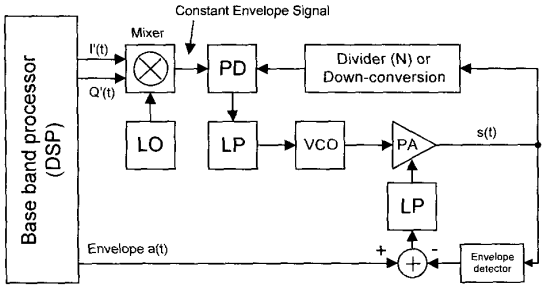

Fig. 2. Polar linearisation for a digital transmitter

The functionality is as follows. The DSP generates an envelope signal, $a(t)$ and two quadrature signals, $I'(t)$, and $Q'(t)$, representing a RF constant envelope signal. The quadrature signals are up-converted and used as reference signal for the phase detector. The necessary extra DSP calculations are as follows:

$$a(t) = \sqrt{I(t)^2 + Q(t)^2} \qquad \text{(EQ 1)}$$

$$I'(t) = \frac{I(t)}{A(t)} \qquad Q'(t) = \frac{Q(t)}{A(t)} \qquad \text{(EQ 2)}$$

where $I(t)$ and $Q(t)$ are the digital modulated signals normally provided by the DSP. The calculations can easily be carried by a modern DSP, if necessary by using table look up techniques. The resulting output of the system figure 2 is as follows:

$$s(t)=A(t)(Re[(I'(t)+J\cdot Q'(t))\cdot e^{J\omega_c \cdot t}]) \qquad \text{(EQ 3)}$$

which is the normal linear modulated signal. In the following the new system will be analyzed.

3. Analysis of the polar linearisation system.

The analysis of the transmitter architecture in figure 2 is based on the signal diagram shown in figure 3. The PA is modelled by a amplitude (AM-AM) and phase (AM-PM) characteristic. The former describes the output amplitude as a function of the control voltage. The latter describes the phase difference between the RF input and output of the PA as a function of the control voltage. The loop dynamics in figure 3 is set by the loop filters F(s) and G(s). For a fixed PA-gain the amplitude and phase feed back loops are described with the following equations.

$$\frac{a_{PA}(s)}{a(s)} = \frac{G_{PA}G_F(s)}{1+BG_{PA}G_F(s)} = H_{AL}(s) \qquad \text{(EQ 4)}$$

$$\Phi_{PA}(s) = H_{Ref}(s)\cdot\Phi_{Ref}(s) + H_{PM}(s)\cdot\Phi_{AMPM}(s) \qquad \text{(EQ 5)}$$

where G_{PA} is the PA-gain, B is the gain of the amplitude detector, $\Phi_{Ref}(s)$ is reference phase provided by the DSP and $H_{PM}(s)$ is the injected phase distortion due to amplitude to phase conversion (AM-PM).

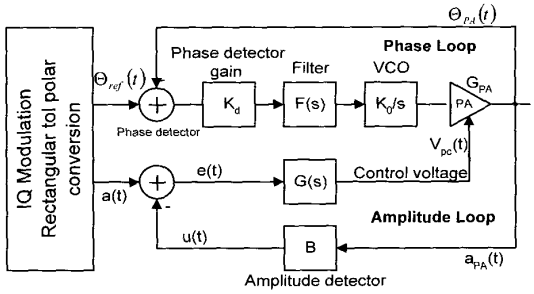

Fig. 3. Polar loop signal model

An overall linear system is achieved if $H_{AL}(s)$ and $H_{Ref}(s)$ are close to one and $H_{PM}(s)$ is close to zero in the band of interest ($f<f_{lin}$). This bandwidth should be chosen to 2-4 times the channel bandwidth, f_{ch}, to be able to attenuated spectral regrowth in the neighbour channels [1].

If we assume that a charge pump is employed within the phase loop, $H_{Ref}(s)$ assumes an ordinary type 2 PLL transfer function [4] and $H_{PM}(s)$ assumes a VCO phase transfer function.

The main problem of using feedback in linearisation systems is that the loop-gain decreases for a decreasing PA-gain. For our PA (figure 4) the PA-gain approaches zero for small and large amplitudes due to compression and turn-off phenomenons. Therefore, the system can only be designed to operate properly in an amplitude interval, where a minimum PA-gain is insured. For a higher order loop filter, $G(s)$, the maximum filter gain is determined by a minimum stability gain margin, and by the maximum PA-gain, $G_{PA,max}$. Therefore the maximum amplitude error $(H_{AL}(s)-1)$ cannot be minimized by choosing an arbitrarily high

filter DC gain, *G(0)*. Another performance limitation of the linearisation system is the delay between the phase, $\Phi_{PA}(t)$, and the amplitude signal $a_{PA}(t)$. The delay of the signals is determined by the closed loop transfer functions $H_{AL}(s)$ and $H_{Ref}(s)$.

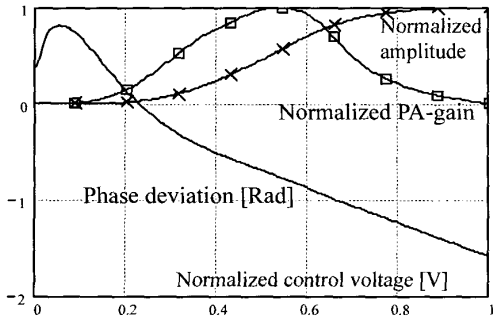

Fig. 4. PA output versus the control voltage

A constant delay difference between these signals could be compensated in the DSP, but a varying delay would require significant DSP processing power. From EQ. 4 we see that the amplitude transfer function varies due to varying PA-gain. The phase transfer function does not depend on the PA-gain and represents a fully linear system.

The bandwidth of amplitude transfer function varies between the bandwidth of the loop filter, f_g, and a bandwidth approximately L times larger. Where L is the loop-gain. To insure a low variation of the group delay a minimum bandwidth of the closed loop system, $H_{AL}(s)$, must be guaranteed. E.g. if a first order loop filter, G(s), with one pole (f_g) and a DC gain of G_0 is used, the closed loop system is of first order, with a minimum bandwidth depending on the filter pole and the minimum PA-gain.

$$f_{CL,min} = (1 + BG_{PA,min}G_0)f_g \qquad \text{(EQ 6)}$$

The group delay is as follows

$$\tau(f, f_{CL}) = f_{CL}/(2\pi(f^2 + f_{CL}^2)) \qquad \text{(EQ 7)}$$

The group delay is nearly frequency independent if the closed loop bandwidth, f_{CL}, is significantly larger than the band of interest (f_{lin}).

$$\tau(f) \cong \tau_{max} = 1/(2\pi f_{CL,min}) \qquad \text{(EQ 8)}$$

A constant group delay results in a delayed but undistorted amplitude signal. The RF signal will, however, be distorted because of the time offset between the amplitude and phase signal. The amount of distortion also depend on the type of modulation. To relate the delay and the distortion, we calculated the distortion as a function of the delay for a long GSM/EDGE modulated [5] signal (figure 5)

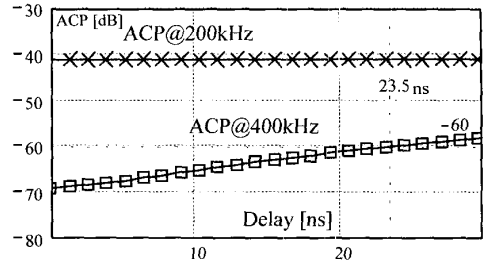

Fig. 5. ACP versus amplitude delay

We found that the ACP (spectral leakage) requirements were more restrictive than the EVM (inband signal quality) requirements (EVM<9%). In figure 5 a graph is showing ACP at an offset of 200kHz and 400kHz. They are required to be below -30dB and -60dB [5] respectively. So the maximum allowable delay is 23.5ns corresponding to an ACP of -60dB at an offset of 400kHz. Based on a minimum PA-gain, EQ. 6 and EQ. 8 and the relation in figure 5, an estimate for the minimum allowable filter bandwidth can be found.

4. Gain compensation

In the previous section we showed that the bandwidth and loop-gain is a function of the PA-gain which again is a function of the amplitude of the modulated signal. For higher order systems, it's not possible to chose the loop-gain arbitrarily high due to stability reasons. It is necessary to trade of bandwidth and loop-gain for gain stability margin.

To compensate for the varying gain in amplitude loop, we suggest to insert a variable gain stage after the calculation of the error, $e(t)$ (see figure 6). Based on the PA-gain and the amplitude, the gain of the variable gain stage can be controlled to stabilize the loop-gain.

The gain compensation signal can be realized either as an two quadrant Gilbert multiplier or as an op-amp gain stage where the feedback resistance consist of an array of switched resistors. In the former case a simple D/A converter would be required. In the latter case the gc(t) would be a n-bit bus controlling the switches

In both cases high precision of the gain value is not required as long as the loop-gain is kept high. This means that the linearisation system is insensitive to deviations of the PA-gain e.g. due to aging and temperature variations. The gain compensation can also be non-linear without affecting the system linearity..

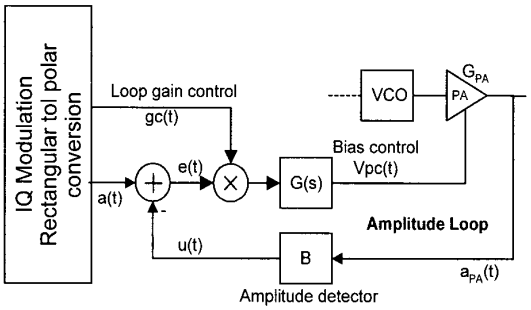

Fig. 6. Linearisation system DSP controlled gain

The gain control signal, *gc(t)*, could be based on a sample measurement of one PA because only an approximate value is required for the compensation.

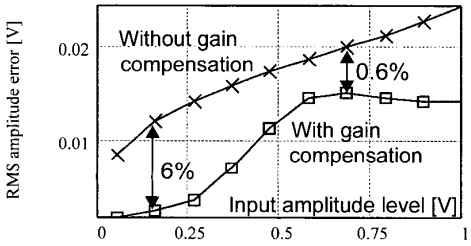

Fig. 7. RMS amplitude error w. and w.o. gain compensation versus maximum amplitude level.

To insure a low complexity of the D/A converter between the DSP and the multiplier the gain control signal should be quantized. The amplitude is mapped to intervals with an associated gain compensation value. The intervals and the gain control values should be chosen, so that the PA-gain times the gain control value has a minimum variation for all amplitudes. The actual gain values can be stored in a look-up table inside the DSP. The signal used for look-up is the amplitude which is already available in the DSP.

To demonstrate the principle, we simulated an amplitude loop with and without a gain control. We used the PA specified in figure 4. The gain control values were quantized to 4 bits with a minimum value of 1 and maximum value of 5. The maximum DC loop-gain was 20 and the filter pole was set to 1 MHz for both systems. The RMS amplitude error versus the maximum amplitude is shown in figure 7. An improvement is observed for all amplitude levels even though both systems have the same maximum loop-gain and stability margin. For low amplitudes we observe an improvement on more than 6% RMS.

5. Conclusion

A new architecture for polar linearisation of RF power amplifiers suitable for digital transmitters was presented. The number of power consuming analog signal processing blocks were reduced and moved to the digital domain (DSP). Furthermore, an extension to the new architecture that reduces the stability constraints and maintains a constant loop-gain and system bandwidth was introduced. Simulations showed the reduction in the amplitude error was more 6% for low amplitude levels.

The distortion sensitivity to delay difference in the signal path of the phase and amplitude was analyzed, and simulations showing the relation between delay and ACP were shown. Guidelines for the loop bandwidth was given. The simulations based on a radio system (GSM/ EDGE) that supports amplitude and phase modulation were presented. Signal quality (EVM) and spectral regrowth (ACP) were simulated based on a measured power amplifier.

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A 29dBm 1.9GHz Class B Power Amplifier in a digital CMOS Process

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Abstract: A two stage class B power amplifier for 1.9 GHz is presented. The amplifier is fabricated in a standard digital CMOS process with low resistivity substrate. The output power is 29dBm in a 50 Ohm load. A design method, based on sweeping the loss and the resonance frequency of a LC tank to determine large signal parameters of the output transistor, is presented. Based on this method proper values for on-chip interstage matching and off-chip output matching can be derived. Measurement of a fabricated chip is compared with the simulated circuit.

1. Introduction

The continuing reduction in production cost and the fast improvement of technology within personal communication systems makes it possible to extend the market and reach most people. The CMOS technology has played an important role in providing high functionality and complexity at low costs. For cheap wireless terminals it is attractive to integrate the RF front-end with the back-end signal processing to reduce assembly cost. Also if expensive RF technologies such as GaAs could be avoided in the design, costs could be reduced. For RF power amplifiers the problem is even more severe due to the limited voltage handling capability (breakdown). The reason that the integration has not been achieved is due to the lack of RF CMOS performance. The linearity and power efficiency seems to be lower given a certain power budget.

If the linearity problem could be solved, the front-ends could be integrated, maybe at the price of a lower power efficiency.

This is the motivation for the present work. We want to design a power amplifier that supports linear modulations schemes such as QPSK either by possessing the linearity, or by accommodating linearization techniques, such as Cartesian Modulation feed back, to enhance the linearity. The foundation for being able to utilize linearization techniques is that the PA itself is fairly linear to insure stability.

In this paper we describe a class B power amplifier (PA) implemented in a mainstream digital CMOS technology. Opposed to class E amplifiers, which have got a lot of attention lately [2] due to a good power efficiency, class B amplifiers are inherently more linear.

This text is divided into the following chapters. Chapter 2 discusses limitations of CMOS power amplifiers. Chapter 3 describes the power transistor and the matching network. Chapter 4 describes the gain stage, the interstage matching network and passives. Chapter 5 deals with the layout. Chapter 6 presents measurements of the fabricated chip and chapter 7 draws the final conclusions.

2. Limitations in a CMOS process

The power amplifier output stage is limited by the following factors.

The first important factor is the limitation in the CMOS processes due to the low gate oxide break down voltage (~5V for 5nm gate oxide). This voltage limits the maximum gate-drain voltage and thereby the maximum supply voltage. Depending on the class of operation (B,C,E) of the output stage, the relation between the maximum drain voltage and the supply voltage varies. For class B operation the ratio is 2, whereas for class E the ratio is 2-5

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[6]. Therefore, a class E amplifier requires a lower supply voltage for the same breakdown voltage.

The second limitation is the low output impedance of the PA. To achieve a high output power, a low effective resistive load must be chosen. The result is a high sensitivity to parasitic resistance in the matching circuits and a complicated matching circuit due to a higher transformation ratio.

The third limitation of the output stage is the maximum PA output current needed to achieve the required power in the load. The current may be so high that electromigration and parasitics in the circuit cause performance degradation.

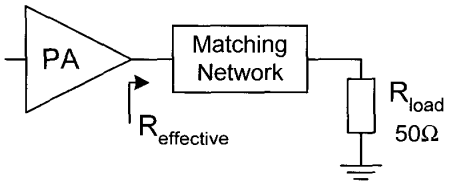

Fig. 1. Power amplifier and load

3. Designing the output stage

Due to the linearity and the capability to operate at low supply voltages a class B output stage is chosen. A method to find the optimum load and the large-signal effective drain-source capacitance is described.

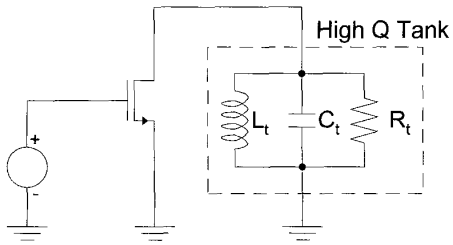

Fig. 2. Determination of effective transistor load using a high Q tank.

The size of the output transistor is determined using the circuit shown in figure 2. A high Q tank is used as load which eliminates the effect of the drain-source capacitance. Furthermore the tank filters the harmonic of the carrier frequency so a load for the carrier frequency is found. A simulator which takes large signal nonlinearity into account is used. Harmonic balance or transient simulation are suited. A bias voltage corresponding to the threshold voltage of the transistor is required for class B operation. The RF voltage swing should be chosen large enough to allow the transistor to get close to the triode region. This can be determined from a standard Ids-Vgs plot.

Sweeping the LC tank-loss, the optimum large signal working condition can be found. Such a sweep is depicted in figure 3. By varying the transistor width and sweeping the tank loss, the load for optimal output power or power efficiency is found.

For an output power of 1 Watt, a width of 10000µm and a drain efficiency of 68% was achieved. The efficiency should of course be taken with cautions as losses in the matching network are neglected. The amplitude of the gate signal was 1 Volt which can easily be provided by a driver stage as the supply voltage is 3 Volt.

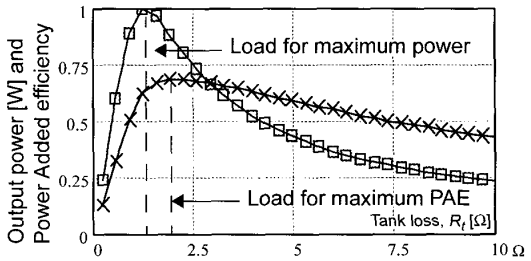

Fig. 3. Normalized output power (square) and PAE (cross) versus tank loss

If the Q value of the tank is lowered (5-10) so the influence of the drain-source capacitance can not be neglected, a displacement in frequency of the optimum load is observed. Then the frequency displacement can be used to calculate the large signal drain-source capacitance the following way:

$$C_{ds,\,effective} \cong 2 \cdot \frac{Q}{R \cdot \omega_c} \cdot \left(\frac{\omega_{peak}}{\omega_c} - 1 \right) \quad \text{(EQ 1)}$$

Now a large signal model for the output transistor is available in the sense that a optimum restive load and an effective drain-source capacitance is available. If the matching network establishes the effective resistance and cancels the calculated effective drain-source capacitance, the required RF operation of the transistor is insured. The design of a matching circuit for the 50 Ohm load is now a simple matching exercise.

4. Gain stage and interstage matching

In this design a 0.25μm CMOS process is used. This process provide sufficient gain to achieve the desired gain of 20 dB with two stages (figure 4). In order to control the DC bias voltage of the output transistor independently from the drain voltage of the input transistor, a big capacitor (20pF) is inserted. The parasitic capacitance to the substrate will be significant, because the actual capacitor requires a large area as thin oxide MIM capacitors are not available.

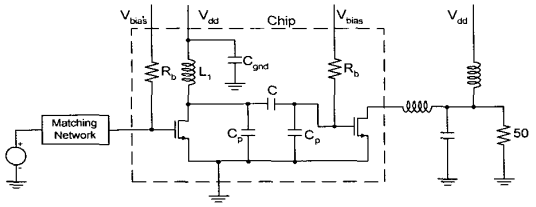

Fig. 4. PA circuit

The on-chip inductor resonates out the parasitic capacitance consisting of the gate capacitance of the output transistor and the parasitics of the on-chip DC block capacitor. A simple but realistic inductor model derived from the current sheet model [4] was used in the design phase, which made it possible to find the inductor within a few iterations. Below the inductor, a grounded poly shield [5] (see chip photo figure 6) was placed to prevent capacitive coupling to the low resistivity epi-substrate. The final inductor was verified by the inductor simulator program, ASITIC, and showed agreement within 5% of the simple model.

The input transistor operates in class A and is sized to cancel the losses of the inductor and to provide a voltage swing of 1V on the gate of the output transistor (section 3). The bias voltage is provided though a 400 Ohm on-chip resistor to avoid loading the AC signal on the gate.

5. Layout

The layout (figure 5) of the PA was in 0.25μm, 6 metal layers CMOS process. Two area demanding capacitors are used. The DC block capacitor in the middle of the layout was realized as lateral flux capacitors in metal 3 and metal 4, whereas metal 5 and 6 were layed out as plates on top.

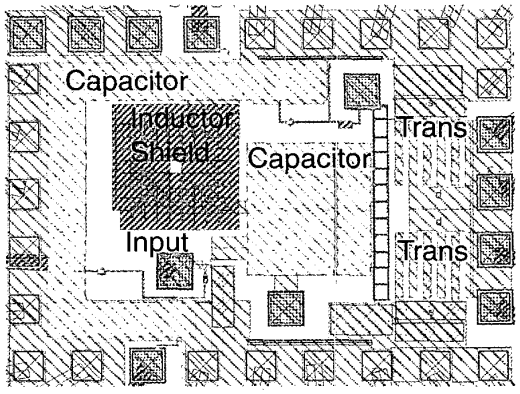

Fig. 5. Layout of the PA

The reason why lateral flux capacitors were used for metal 3 and 4 is that the spacing between adjacent metal is smaller (0.4μm) than the spacing between two different metal layers (0.9μm). Utilizing metal layer 3,4,5 and 6, one achieve capacitance density of approximately 0.19 fF/μm^2. Metal layer 1 and 2 are not used to limit the coupling to the substrate. The DC block capacitor is approximately 20pF. The grounding capacitor, C_{gnd}, in figure 4 is realized using all metal layers. The density of this capacitor is approximately 0.39 fF/μm^2. The total capacitance is 46 pF. The output transistor is folded to minimize the drain and source area. The maximum width of each folded transistor is 12μm to insure a small gate resistance and thereby a fast transistor. Also after every 5th transistor, a column of substrate contacts is inserted to insure a low resistance to the substrate. The ground bonding inductance should be minimized using many ground pads and bonding wires. In this design 19 ground pads were used.

The on-chip inductor was realized in metal layer 6 with a poly shield to shield against capacitive coupling to the substrate (see chip photo in figure 6)

6. Simulations and measurement

A printed circuit board (PCB) was designed and the bare PA-chip was glued directly on the print and bonded (chip on board). Thereby the shortest possible bondwires were achieved. The

maximum output power was measured to 29.2 dBm (table 1) at the frequency of 1.95 GHz.

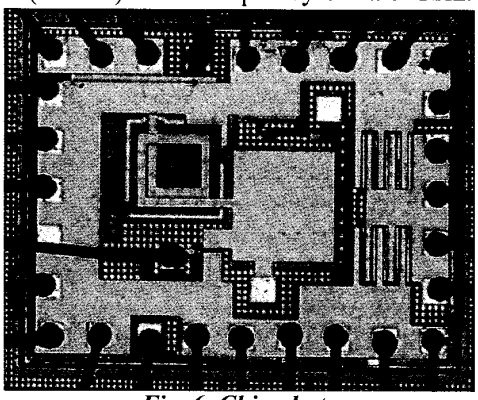

Fig. 6. Chip photo

The small signal power gain was 20.7 dB and the power added efficiency was 27.4%. A power sweep is shown in figure 7.

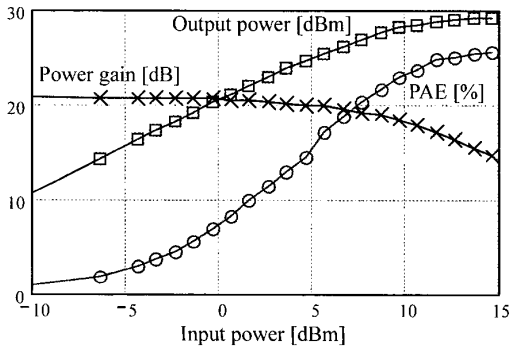

Fig. 7. Measured PA characteristic

The initially simulated output power was 1W and the maximum measured output power was 0.84W. The difference is due to PCB parasitics such as wire inductance and wire capacitance. Furthermore the discrete components in the matching network causes deviations. We model the PCB wires with strip lines and the components in the matching network with finite Q models and achieved a result within 5% of the measured output power.

7. Conclusion

A 1.9GHz class B power amplifier was designed in a digital mainstream 0.25μm CMOS process. The designed and fabricated PA delivered an output power of 29.2 dBm (0.84W) which to our knowledge is the best result for a class B CMOS power amplifier [1][2][3][7]. Agreement between measurement and simulation was achieved by carefully model wires and discrete components of the PCB. A design method based on deriving large signal parameters of the output transistor using an LC tank was presented. The design of the passives, on-chip inductor and lateral flux capacitors were described.

Table 1. PA characteristic

Property	Value
Process	0.25μ CMOS
Supply voltage [V]	3
Frequency [GHz]	1.95
Max Power [dBm]	29.2
PAE [%]	27.4
small signal gain [dB]	20.7
large signal gain [dB]	14.2

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